
# *Model 625A*
# *CW Microwave Counter*
## *Operation and Service*

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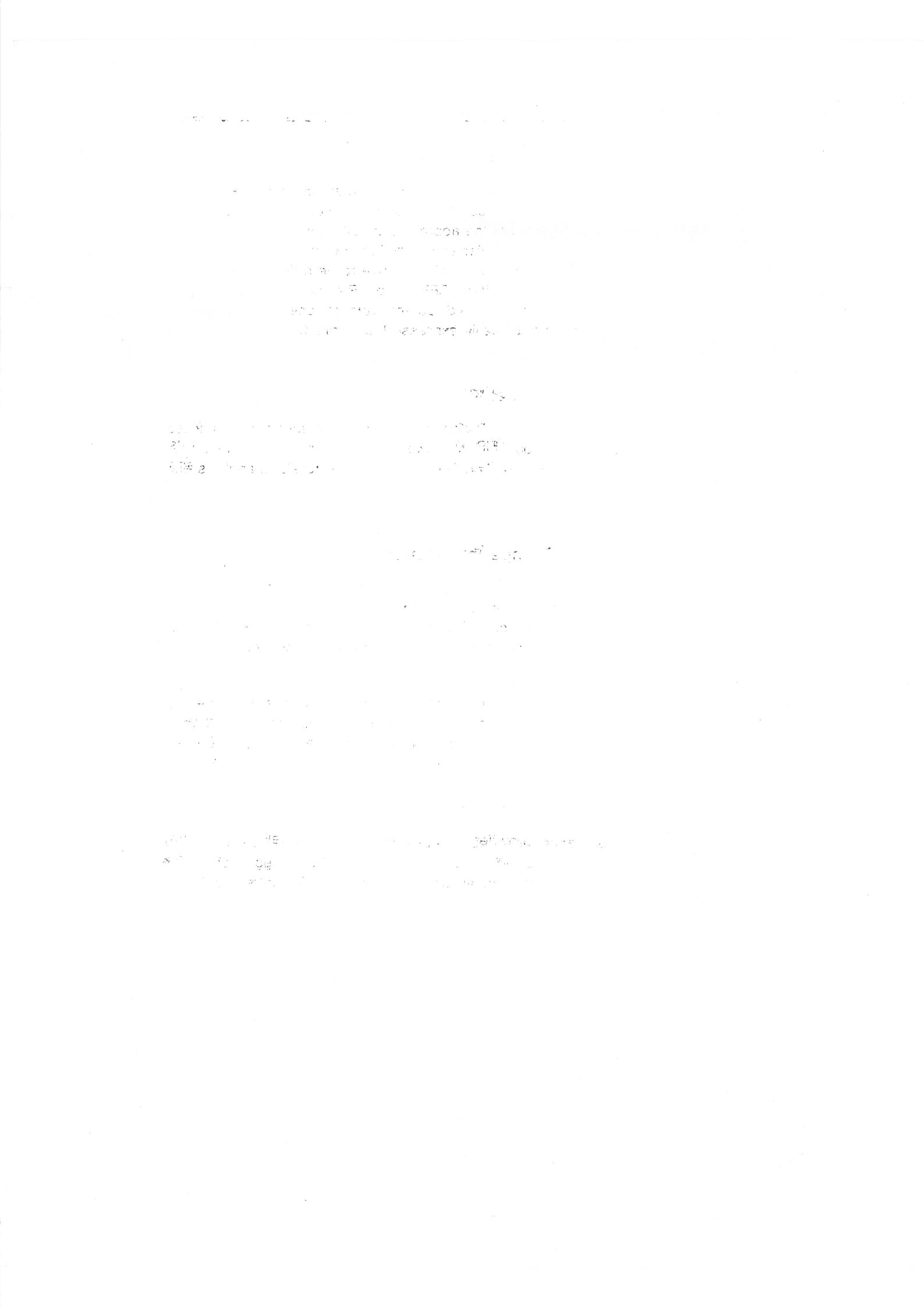
Manual Assembly Part Number: 5585035-01
Manual Text Part Number: 5580075-01
Printed in U.S.A., October 1990


CCN: 8004



## Warranty

EIP Microwave, Inc. warrants this product to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level is not covered by the warranty. Removal, defacement, or alteration of any serial or inspection label, marking, or seal may void the warranty. EIP Microwave, Inc. will repair or replace, at its option, any components of this product which prove to be defective during the warranty period, provided the entire unit is returned PREPAID to EIP or an authorized service facility. In-warranty units will be returned freight prepaid; out-of-warranty units will be returned freight collect. No warranty other than the above is expressed or implied.

## Certification

EIP Microwave, Inc. certifies this instrument to be in conformance with the specifications noted herein at time of shipment from the factory. EIP Microwave, Inc. further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology.

## Manual Change Information

As EIP continually improves and updates its products, changes to the material covered by the manual will occur. When a part or assembly in an EIP instrument is changed to the extent that it is no longer interchangeable with the earlier part, the configuration control number (CCN) of the instrument, shown on the title page of the manual, will change, and a new edition of the manual will be published.

To maintain the technical accuracy of the manual, it may be necessary to provide new or additional information with the manual. In these cases, the manual is shipped with a Manual Update. Please be sure to incorporate the information as instructed in the Manual Update.

## Customer Suggestion Form

A mail-in form at the end of this manual provides an easy way for you to tell us about any additions, corrections, or changes that would improve this publication. Your suggestions are a valuable part of the input used in revising our manuals and developing the structure and format for new manuals.

# SAFETY

The EIP model 625A is a Safety Class 1 instrument. This instrument has been designed and tested according to international safety requirements. This manual contains information, cautions, and warnings that must be followed by the service person to ensure safe operation and to retain the instrument in safe condition.

## SAFETY SYMBOLS

**WARNING** The WARNING sign denotes a hazard. It calls attention to a procedure or practice, which, if not correctly performed or adhered to, could result in personal injury.

**CAUTION** The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

## OVERALL SAFETY CONSIDERATIONS

**WARNING**

Before this instrument is switched on, the protective earth terminals of this instrument MUST be connected to the protective conductor of the ac power cord. The power cord shall only be inserted into a receptacle provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective earth (grounding) conductor.

**WARNING**

Only fuses with the required rated current voltage and specified type should be used. DO NOT use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

**WARNING**

Whenever it is likely that the protection has been impaired, the instrument MUST BE made inoperative and be secured against any unintended operation.

**WARNING**

All protective earth terminals, extension cords, autotransformers, and devices connected to this instrument should be connected to a socket outlet provided with a protective earth contact. Any interruption of the protection will cause a potential shock hazard that could result in personal injury.

**WARNING**

Whenever ac power is connected to this instrument, the power supply is energized. Therefore, exercise caution whenever covers are removed.

**CAUTION**

Before connecting power to the instrument, check to insure that the correct fuse is installed and the voltage select switch on the rear panel of the instrument is set properly. Refer to Section 2, Installation.

**CAUTION**

Excessive signals can damage this instrument. To prevent damage, do not exceed specified damage level. Refer to specifications listed in Section 1.

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# SECTION 1
# GENERAL INFORMATION

## DESCRIPTION

The EIP 625A is a microprocessor-based microwave frequency counter that measures the frequency of CW signals from 10 Hz to 20 GHz.

Frequency measurements are divided into three bands. Band 1 is a high impedance input (1 Megohm/20 pF) and covers the frequency range from 10 Hz to 100 MHz, with a sensitivity of 25 mV rms. Band 2 has an input impedance of 50 ohms and covers the frequency range from 100 MHz to 1 GHz, with a sensitivity of -15 dBm. Band 3 has an input impedance of 50 ohms and covers the frequency range from 950 MHz to 20 GHz, with a sensitivity of -25 dBm from 950 MHz to 12.4 GHz and a sensitivity of -20 dBm from 12.4 to 20 GHz.

Through keyboard control, the EIP 625A counter provides frequency offsets and frequency multiplication. Remote operation via the general purpose interface bus (GPIB) is a standard feature. A high stability time base is available as an option. Measurements are presented on a 12 digit LED display that is sectionalized to read directly in GHz, MHz, kHz, and Hz.

## SPECIFICATIONS

| General | |
|---|---|
| Size (H, W, D) | 3.5 in. x 8.125 in. x 18.5 in. (8.9 cm x 20.6 cm x 47.0 cm) |
| Operating Temperature | 32° to 122° F (0° to 50° C) |
| Environmental | Mil-STD-46IC and Mil-T-28800D Type III, class 5, style E |
| Power | 100/120/140/200/220/240 Vac ±10%, 50-400 Hz, 60 VA typical |
| Resolution | 1 Hz to 10 MHz in Band 1<br>1 Hz to 1 GHz in Bands 2 and 3 |
| Gate Time | |
| Band 1 and 3 | 1 ms to 1 s (depending upon resolution) |
| Band 2 | 4 ms to 4 s (depending upon resolution) |

| Band 1 | |
|---|---|
| Frequency Range | 10 Hz to 100 MHz |
| Connector | BNC (female) |
| Impedance | 1 M ohm/20 pF, nominal |
| Sensitivity | 25 mv rms, 15 mv rms typical |
| Maximum Input | 1 V rms |
| Damage Level | 100 V rms |
| Maximum FM | Carrier frequency must remain within band |

| Band 2 | |
|---|---|
| Frequency Range | 100 MHz to 1 GHz |
| Connector | BNC (female) |
| Impedance | 50 ohms, nominal |
| Sensitivity | -15 dBm, -20 dBm typical |
| Maximum Input | +10 dBm |
| Damage Level | +24 dBm |
| Maximum FM/Chirp | Carrier frequency must remain within band |

| Band 3 | |
|---|---|
| Frequency Range | 950 MHz to 20 GHz |
| Connector | Precision Type N (female) |
| Impedance | 50 ohms, nominal |
| VSWR | 2.5:1, typical |
| Sensitivity | -25 dBm (950 MHz to 12.4 GHz) -30 dBm, typical<br>-20 dBm (12.4 to 20 GHz) -25 dBm, typical |
| Maximum Input | +10 dBm |
| Damage Level | +45 dBm peak (30 watts) continuous power. +53 dBm peak (200 watts) pulsed power ($\leq$1 µs pulse width, 0.1% duty cycle). |
| Amplitude Discrimination | 10 dB. If <10 dB, will count one signal accurately if separated by >200 MHz. |
| Maximum FM/Chirp | 20 MHz peak-to-peak (up to 10 MHz rate) |
| Acquisition Time | <220 ms standard. <20 ms center frequency mode. |
| Center Frequency | Will lock on signals $\leq$5 MHz from the entered frequency at sensitivity; resolution is 1 MHz. (Equal amplitude signals must be separated by $\geq$40 MHz.) |
| Tracking Speed | $\geq$800 MHz/s |

| TCXO Time Base | |
|---|---|
| Frequency | 10 MHz |
| Aging Rate | $<\lvert 1 \times 10^{-7} \rvert$ per month. $\lvert 1 \times 10^{-6} \rvert$ per year. |
| Short Term Stability | $<1 \times 10^{-9}$ RMS for one second averaging time |
| Temperature Stability | $<\lvert 1 \times 10^{-6} \rvert$ over the range of 0° to 50° C |
| Line Variation | $<\lvert 1 \times 10^{-7} \rvert$ ($\pm$10% line voltage change) |
| Warm-up Time | 30 minutes |
| Time Base Output | 10 MHz, square wave. 1 V peak-to-peak minimum into 50 ohms from rear panel BNC (female) connector. |

| | |
|---|---|
| | TCXO Time Base (Continued) |
| Phase Noise | -95 dBc/Hz at 10 Hz from carrier |
| | External Time Base |
| Input | Requires 10 MHz, 1 V peak-to-peak minimum into 300 ohms be applied at rear panel BNC (female) connector. External time base operation enabled via Special Function 08. |
| | Oven Oscillator Time Base (Option 05) |
| Phase Noise | -95 dBc/Hz at 10 Hz from carrier |
| Aging Rate/24 Hours (After 72 hour warm-up) | $<\|5 \times 10^{-10}\|$ |
| Short Term Stability (1 second average) | $<1 \times 10^{-10}$ rms |
| 0° to +50° C Temperature Stability | $<\|3 \times 10^{-8}\|$ |
| ±10% Line Voltage Change | $<\|2 \times 10^{-10}\|$ |
| Retrace | $<5 \times 10^{-8}$ of final value 15 minutes after counter is plugged in at 25° C if counter is unplugged for less than 10 minutes. |
| External dc Input | Range: 10 to 15 Vdc. Rear panel connector for powering the oven oscillator during transit. A cable for connecting the input to an automobile cigarette lighter is included with the oven oscillator option. |

**CAUTION**

**To avoid damage to the oven oscillator option, connect only +10 Vdc to +15 Vdc to the oven oscillator power input connector on the rear panel.**

# SECTION 2
# INSTALLATION

## UNPACKING AND INITIAL INSPECTION

If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the electrical performance tests, notify EIP in care of the address shown on the title page. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as EIP. Keep the shipping materials for carrier's inspection. The EIP office will arrange for repair or replacement without waiting for claim settlement.

## STORAGE ENVIRONMENT

The instrument may be stored or shipped in environments within the following limits:

Temperature: –40° to +75° C
Humidity: Up to 95%
Altitude: Up to 50,000 feet (15,240 meters)

## OPERATING CONDITIONS

This instrument is designed to be operated at temperatures not exceeding 0° to 50° C at a relative humidity not to exceed 95% (75% over 25° C and 45% over 40° C). This instrument will perform to specifications at altitudes not exceeding 3050 m (10,000 ft) and will tolerate vibrations not exceeding 2 g's. It is fungus resistant. The chassis is not designed to provide protection from mechanical shock or falling water particles and is intended for normal bench use in an environmentally clean area.

## INSTALLATION

There is no special installation required for the EIP 625A frequency counter. The unit is a self-contained bench or rack mounted instrument that only requires connection to a standard, single-phase power line for operation.

## PREPARATION FOR USE

### VOLTAGE SELECTION

**CAUTION**

**Disconnect ac power cord before changing voltage selection switch.**

The voltage selection switch should be set to the proper line voltage. (See Figure 2-1.) To change the line voltage, proceed as follows:

1. Disconnect the counter from the power line.

2. Using a screwdriver, turn the slotted voltage indicator to the desired position.

## FUSE REPLACEMENT

### WARNING

**Disconnect ac power cord before replacing fuse.**

The counter has one fuse located on the rear panel, above the line voltage plug. The type of fuse used in your counter depends upon the primary power, as follows:

| Line Voltage | Fuse Type |
|---|---|
| 100/120/140 Vac | 1.5 A, slow-blow, MDL |
| 200/220/240 Vac | 0.8 A, slow-blow, FST |

To release the fuse, use a screwdriver to rotate the slotted cap counterclockwise. To reinstall the fuse, press the fuse and slotted cap assembly into the fuse cavity and turn cap clockwise until it locks into place.

### CAUTION

**To avoid damage to the counter, always be sure that the fuse used is the type and value specified, and that the voltage select switch is set to correspond to the ac power input voltage. (See Figure 2-1.)**

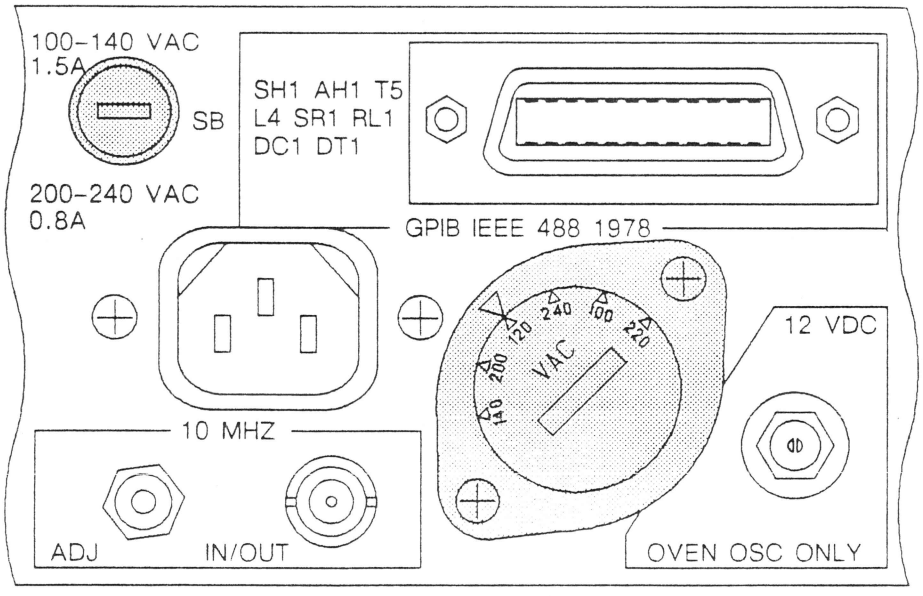



Figure 2-1. Rear Panel Fuse and Voltage Select Switch Locations.

## INCOMING OPERATIONAL CHECKOUT

This following test is designed to provide a basic operational check of the instrument. If more extensive testing is required, refer to Section 5.

1. Before connecting power to the instrument, check to make sure the correct fuse is installed and the voltage select switch is set properly.

2. Connect the power cord to the appropriate single-phase power source. The ground terminal on the power cord plug must be properly grounded.

3. Turn the POWER switch to on. All LEDs and annunciators should light for about two seconds. The counter model number and GPIB address should be displayed for about one second. The counter should then display all zeros indicating that the automatic self-check has been successfully completed.

4. Press: SPECIAL FUNC (9) (0) (1) — Display should read 100 000 ±1 (100 MHz).

5. Press: SPECIAL FUNC (9) (0) (2) — Display should read all 8's and all annunciators should be lit.

6. Press: SPECIAL FUNC (9) (0) (3) — Each display segment should light in turn (adjustable by the front panel SAMPLE RATE control).

7. Press: SPECIAL FUNC (9) (0) (4) — Each digit should light in turn (adjustable by the front panel SAMPLE RATE control).

This completes the operational checkout procedure.

## SERVICE INFORMATION

### PERIODIC MAINTENANCE

To maintain accuracy, it is recommended that the counter be recalibrated every six months. Other than calibration, no periodic maintenance is required.

**CAUTION**

**Do not attempt repair or disassembly of the microwave converter or time base oscillator assemblies. Such action will void the warranty on the counter. Contact EIP or your sales representative if these units require servicing.**

### COUNTER IDENTIFICATION

The counter is identified by three sets of numbers: the model number, a serial number, and a configuration control number. These numbers are located on a label affixed to the frame at the rear of the counter and must be included in any correspondence regarding your counter.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment:

- Name and address of owner.
- Model number, serial number, and configuration control number of the counter.
- A complete description of the problem. (E.g., under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment also experience failure symptoms?)
- Name and telephone number of someone familiar with the problem who may be contacted by EIP for any further information if necessary.
- Shipping address to which the counter is to be returned. Include any special shipping instructions.

## SHIPPING INSTRUCTIONS

Wrap the counter in heavy plastic or kraft paper and repack in original container if available. If the original container cannot be used, use a heavy (275 lb test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of this document.

# SECTION 3
# OPERATION

## INTRODUCTION

This section lists the controls, connectors, and indicators featured on the EIP 625A frequency counter, explains how each counter function operates, and provides some general measurement considerations.

## FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

Front panel controls, indicators, and connectors fall into four general groups: data display, status display, signal input, and keyboard. (See Figure 3-1.)

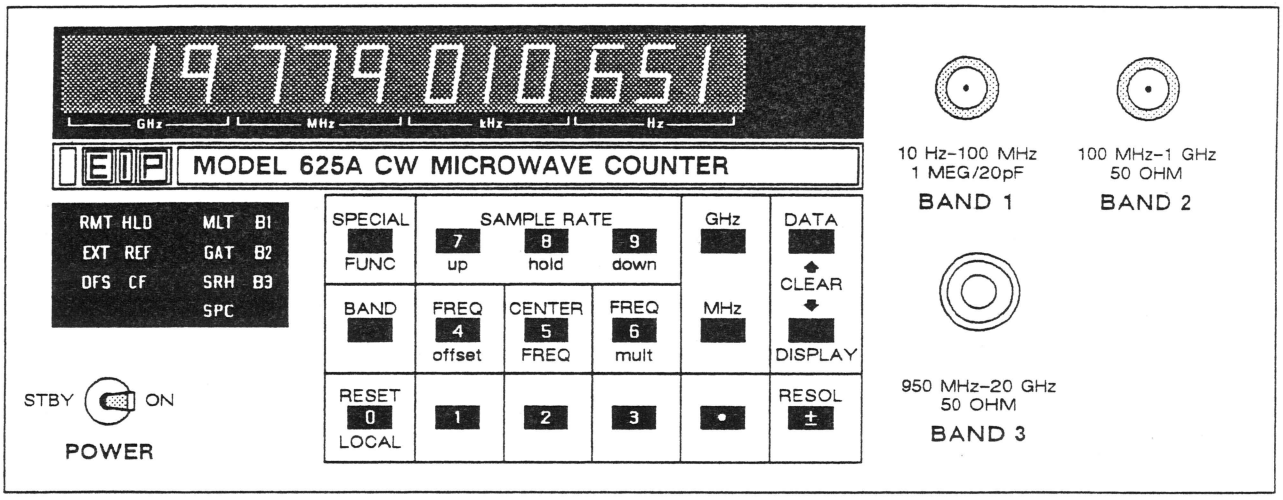



**Figure 3-1. Front Panel Controls, Indicators, and Connectors.**

### POWER SWITCH

- STBY – In standby (STBY) position, all controls and displays are inactive; the Power Supply (A2) is energized, but power is only applied to optional oven time base (if installed).
- ON – In the ON position, power is applied to the counter circuits and controls.

### DATA DISPLAY

The 12 digit LED data display provides a direct numerical readout of an input frequency measurement. The frequency readout is displayed in a fixed position format that is sectioned into GHz, MHz, kHz, and Hz.

### STATUS INDICATORS

- RMT – Lights to indicate that the counter is being controlled via GPIB and all front panel controls are disabled except POWER switch and LOCAL switch.
- EXT REF – Lights to indicate that the counter is set to an external time base reference.
- OFS – Lights to indicate that the frequency offset function is active.
- HLD – Lights to indicate that the counter's measurement cycle is halted. The instrument continues to display the last measurement.

- CF – Lights to indicate that the center frequency function is active.
- MLT – Lights to indicate that the frequency multiplying function is active.
- GAT – Lights to indicate that the counter gate is open and a measurement is being made.
- SRH – Lights to indicate that the counter is in Band 3 and searching for a signal.
- SPC – Lights to indicate that the counter is operating in a special function mode.
- B1 – Lights to indicate that Band 1 has been selected.
- B2 – Lights to indicate that Band 2 has been selected.
- B3 – Lights to indicate that Band 3 has been selected.

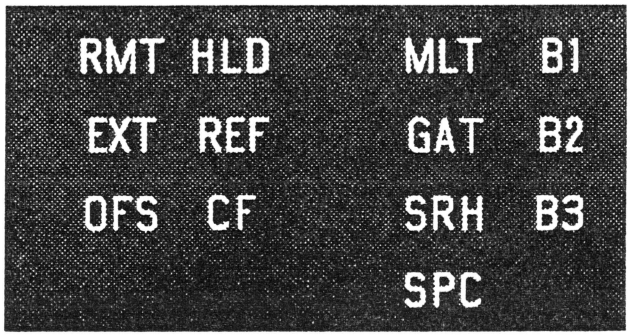



**Figure 3-2. Status Indicators.**

## SIGNAL INPUT CONNECTORS

- BAND 1 – A BNC female connector with a nominal input impedance of 1 megohm shunted by 20 pF.
- BAND 2 – A BNC female connector with a nominal input impedance of 50 ohms.
- BAND 3 – A precision N female connector with a nominal input impedance of 50 ohms.

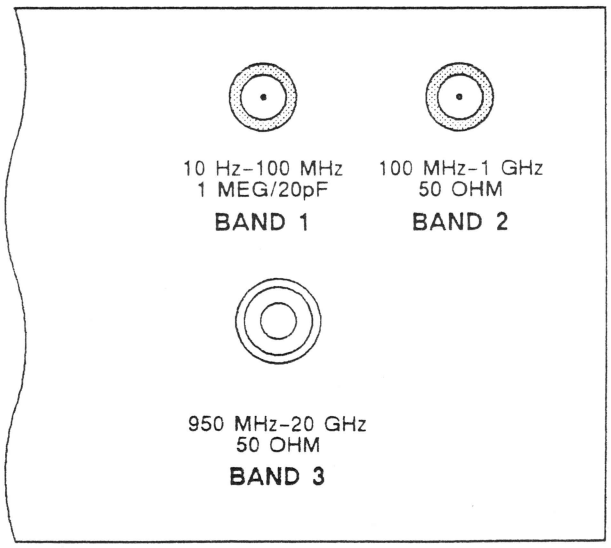



**Figure 3-3. Signal Input Connectors.**

KEYBOARD

Both data entry and function selection are controlled through the keyboard. (See keyboard section on page 3-4.)

## REAR PANEL CONNECTORS AND CONTROL (see Figure 3-4)

- Fuse - Provides overload protection.
- Ac power connector - Input for ac power.
- VAC switch - Sets the operating voltage of the counter to match ac power line voltage.
- 10 MHz IN/OUT - The time base input/output (IN/OUT). This BNC female connector accepts an external time base reference input or provides time base reference output to external units. The state is selectable using Special Functions 07 and 08. (See special functions listing.)
- 10 MHZ ADJ - Provides a means for calibrating the internal oven oscillator frequency. (Option 05 only.)
- GPIB connector - Used for remote operation with General Purpose Interface Bus.
- 12 VDC input - Input for external +12 Vdc source to power oven oscillator during transit. Refer to specifications prior to use of this feature. (Option 05 only.)

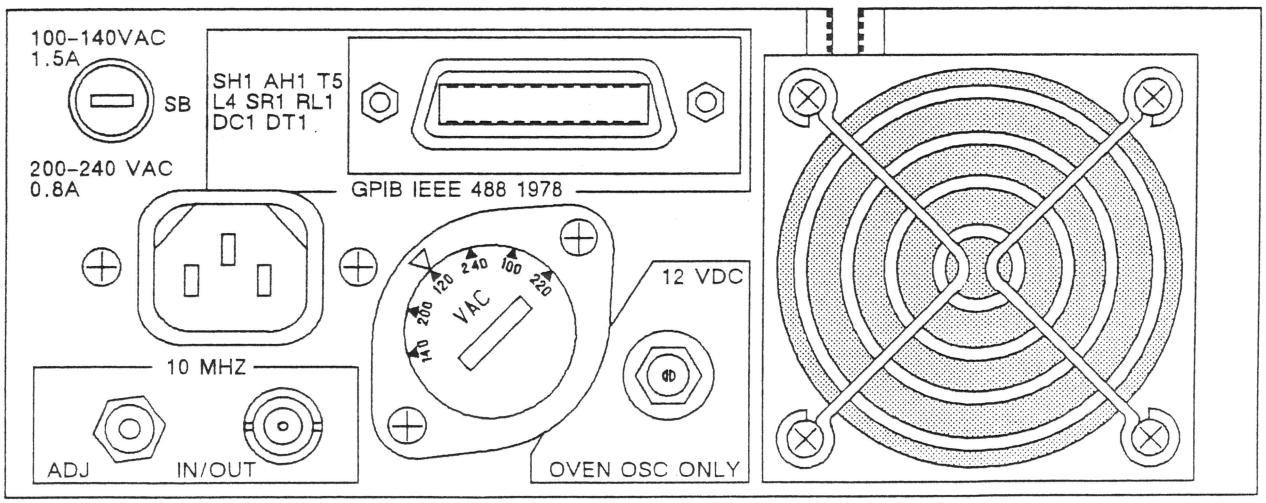



Figure 3-4. Rear Panel Connectors and Control.

## OPERATION

### CAUTION

**The EIP 625A counter is a sensitive measuring instrument. To avoid damage to the instrument, do not exceed the maximum input specifications.**

## POWER ON

With the counter plugged in and the POWER switch set to STBY, displays and controls are inactive. Power is applied only to the optional oven time base, if installed.

When the POWER switch is set to ON, the counter goes through power-up test of RAM and PROM and verification of counter functional operation. Counter displays "EIP 625A" during this test. If all tests are passed, the counter begins normal measurement operation. If any part of the test fails, an error message will be displayed. (See Error Messages section.)

## DEFAULT SETTINGS

When the counter is initially turned on, its state is determined by the default values stored in memory. The factory set default values are shown below. Special Function 72 can be used to customize the power-on default values to meet specific requirements.

| Parameter | Default Value |
|---|---|
| Band | 3 |
| Center frequency | 0 (disabled) |
| Display | Enabled |
| Internal reference | On |
| External reference | Off |
| Frequency multiply | 1 |
| Frequency offset | 0 |
| Hold | Off |
| Resolution | 0 (1 Hz) |
| Sample rate | Maximum |

## KEYBOARD OPERATION

The keyboard consists of 18 pushbutton keys that control the major functions of the counter. Twelve keys are used for numerical data entry—the digits 0 through 9, the decimal point, and the change sign (±). The decimal point key is also used as a trigger (see page 3-5). Two keys (MHz and GHz) act as terminators for the input of frequency parameters. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data, respectively. Each of five of the numerical keys are dual function keys used to select the band, resolution, test function, frequency offset, and frequency multiplier functions.

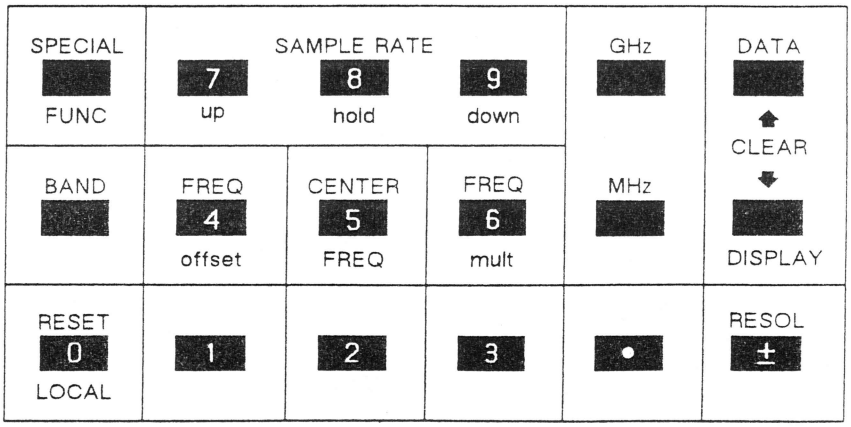



**Figure 3-5. Keyboard.**

### Single Key Instructions

1. Valid Single Key Instructions:

   - RESET LOCAL – If under front panel (local) control, pressing this key halts the counter measurement or acquisition sequence and initiates a new acquisition sequence. It does not affect the status of any measurement condition set by the front panel controls. If under GPIB control (RMT indicator on), pressing this key returns control to the front panel and initiates a new acquisition sequence.

   - CLEAR DISPLAY – If the counter is in the data entry mode, pressing this key clears the current entry and returns the counter to the display measurement. It does not affect stored data. Otherwise there is no effect.

   - SAMPLE RATE up – A single press of this key increases the sample rate one increment. Holding the key down continues increasing the sample rate until maximum sample rate is achieved. At maximum sample rate, the time between samples is 40 ms, nominal.

   - SAMPLE RATE down – A single press of this key decreases the sample rate one decrement. Holding the key down continues decreasing the sample rate until the minimum sample rate is achieved. At minimum sample rate, the time between samples is 10 seconds, nominal.

   - SAMPLE RATE hold – Pressing this key puts the counter sample rate into hold, freezes the display on the last measurement made, and lights the HLD indicator.

   - "." (trigger) – If the counter SAMPLE RATE controls are set to hold, pressing this key once generates a single measurement or special function event.

2. Invalid Single Key Instructions:

   GHz, MHz, CLEAR DATA, all numbers, and ± are invalid single key instructions. None of these keys initiates a single or multiple key instruction. All require a prior key to initiate a valid instruction set. The counter will display ERROR 01 until CLEAR DISPLAY is pressed or a valid instruction set is initiated.

### Multiple Key Instructions

- BAND – The BAND key initiates the band selection instruction set. Band annunciators B1, B2, and B3 flash until 1, 2, or 3 is selected. Counter operation is not affected until an instruction terminating number is selected. At that time, the counter changes bands, resets, and initiates the proper acquisition sequence for the selected band. Selecting any other number or key causes the counter to display ERROR 10, which is displayed until either a valid instruction set is reinitiated or CLEAR DISPLAY is selected.

  This parameter controls the frequency measurement range. Select the appropriate band according to:

| Band | Range |
|---|---|
| 1 | 10 Hz to 100 MHz |
| 2 | 100 MHz to 1 GHz |
| 3 | 950 MHz to 20 GHz |

Keyboard Example:

PRESS: BAND DATA CLEAR to select default band.

PRESS: BAND 2 to select Band 2.

GPIB Example:

Enter: OUTPUT 718;"**BA**ND 2" to select Band 2.

- FREQ offset - The FREQ offset key initiates entry of a positive or negative decimal number to offset the measured frequency (to 1 Hz resolution). A number is input, and the instruction is terminated by selecting a units terminator (MHz or GHz). The OFS annunciator flashes until the instruction sequence is terminated and then remains lit for as long as the instruction is in effect. The display shows the last offset entered until entry of the first number of the new offset. The new offset is displayed as it is being input. The OFS annunciator remains lit while the instruction set is in effect. Selecting any key other than ±, ., a number, a units terminator, or CLEAR DISPLAY causes the counter to display "ERROR 16," which is displayed until CLEAR DISPLAY is selected or until a valid instruction set is reinitiated. The counter exits this mode of operation when the FREQ offset key and the CLEAR DATA key are selected.

  Frequency offset allows the entry of a negative or positive frequency to 1 kHz resolution into the offset frequency register. This parameter controls the constant B in the formula:

  Displayed frequency = (M x measured frequency) ±B

  where M is the frequency multiplier and B is the frequency offset. Select frequency offset in the range of -99.999 999 GHz to +99.999 999 GHz. The number can be entered in any fixed-point format, with the units terminator that determines the scale of the input number.

  Keyboard Examples:

  PRESS: FREQ offset DATA CLEAR to select the default value.

  PRESS: FREQ offset 1 2 . 3 4 MHz to select a 12.34 MHz value.

  PRESS: FREQ offset ± 0 . 1 2 GHz to select a -0.12 GHz value.

  GPIB Example:

  Enter: OUTPUT 718;"**OF**FSET 12.34 MHZ" to select a 12.34 MHz value.

- FREQ mult - The FREQ mult key initiates entry of a positive integer, between 01 and 99, that is multiplied by the measured frequency. The second digit of the entered number acts as the instruction sequence terminator. The MLT annunciator flashes until the sequence is terminated and then remains lit as for long as the instruction is in effect. The display shows the last multiplier until entry of the first digit of the new multiplier. It shows the new multiplier until the instruction is terminated. To review current multiplier status, press the FREQ mult key. The CLEAR DISPLAY key returns the counter to the multiplied and measured display. If both multiplier and offset functions are used, the counter displays the value derived from the following: (measurement x multiplier) + offset. The counter exits this mode of operation when the FREQ mult key and the CLEAR DATA key are selected.

  Frequency multiplier controls the value of the constant M in the formula:

  Displayed frequency = (M x measured frequency) ±B

  where M is the frequency multiplier and B is the frequency offset. The frequency multiplier must be an integer in the range of 01 to 99.

Keyboard Examples:

PRESS: FREQ mult CLEAR DATA to select the default multiplier value.

PRESS: FREQ mult 0 7 to select a multiplier value of 7.

PRESS: FREQ mult 3 1 to select a multiplier value of 31.

GPIB Example:

Enter: OUTPUT 718;"**MU**LTIPLIER 31" to select a multiplier value of 31.

- RESOL - The RESOL key is used to set the least significant digit of the display. Values of .1 (in Band 1 only) and integers 0 through 9 set the least significant digit as a power of 10 and terminate the instruction set as follows:

| Resolution | Values |
|---|---|
| 0.1 Hz | .1 |
| 1 Hz | 0 |
| 10 Hz | 1 |
| 100 Hz | 2 |
| 1 kHz | 3 |
| 10 kHz | 4 |
| 100 kHz | 5 |
| 1 MHz | 6 |
| 10 MHz | 7 |
| 100 MHz | 8 |
| 1 GHz | 9 |

**NOTE**

When a value of .1 Hz is entered in Band 1, the significance of the digits on the front panel display is shifted left 3 digits. For example, a 9 MHz signal input is displayed as 9 GHz (see Figure 3-6). One digit is displayed to the right of the decimal, and the two right-most digits are blanked out. The display digit to the right of the decimal will be zero until the measurement is updated at the end of the 10 second gate interval. When changing bands, the resolution value is retained except when using a resolution of 0.1 Hz in Band 1. The new resolution, when switching to Band 2 or Band 3, is resolution 0.

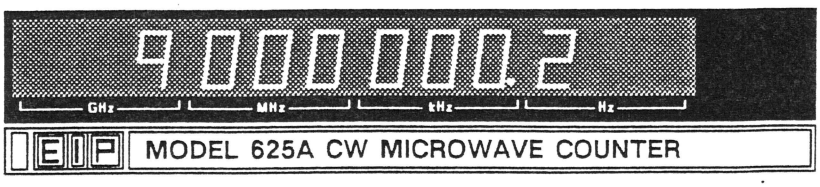



**Figure 3-6. Measurement Display at 0.1 Hz Resolution.**

Keyboard Examples:

PRESS: RESOL CLEAR DATA to select default resolution.

PRESS: RESOL [2] to select resolution 2 (100 Hz).

PRESS: RESOL [.] [1] to select resolution .1 (0.1 Hz).

GPIB Examples:

Enter: OUTPUT 718;"**RE**SOLUTION 4" to select resolution 4 (10 kHz).

Enter: OUTPUT 718;"**RE**SOLUTION .1" to select resolution .1 (0.1 Hz).

- CENTER FREQ - The CENTER FREQ key is used to limit the counter's frequency search range in Band 3, and provides the following capabilities:

  In an environment of multiple signals of equal amplitude (separated by as little as 40 MHz), the counter will select and measure individual signals. The counter will also select and measure a signal among other higher amplitude signals, with the provision that signal separation be greater than 40 MHz. Once a signal is found and measured, and the signal drifts out of the center frequency search range, the counter will track and measure the signal. The center frequency function also shortens the counter's signal acquisition time, thereby providing measurement results more quickly.

  To initiate the center frequency feature, press the CENTER FREQ key, followed by the desired signal frequency (±5 MHz) and a units key (MHz or GHz). To exit the center frequency mode, press the CENTER FREQ key followed by the CLEAR DATA key.

  Keyboard Examples:

  PRESS: CENTER FREQ, CLEAR DATA to select the default value.

  PRESS: CENTER FREQ [1] [4] [.] [8] GHz to select a center frequency value of 14.8 GHz.

  PRESS: CENTER FREQ [2] [1] [7] [5] MHz to select a center frequency value of 2175 MHz (2.175 GHz).

  GPIB Example:

  Enter: OUTPUT 718;"**CE**NTERFREQ 14.8 GHZ" to select a center frequency of 14.8 GHz.

## SIGNAL MEASUREMENTS

### AUTOMATIC FREQUENCY MEASUREMENTS

To measure the frequency of a CW signal, apply the signal to the input connector that corresponds to the frequency being measured and select the appropriate band. The counter automatically finds the signal, measures it, and displays the measured frequency.

### FREQUENCY MEASUREMENT IN A MULTIPLE SIGNAL ENVIRONMENT

In many applications, there is often more than one signal present. In a multiple signal environment, the counter automatically measures the frequency of the highest amplitude signal, within the limitations of the counter's amplitude discrimination specification. Amplitude discrimination is the ability of the counter to select, among multiple signals, the signal of highest amplitude.

It is sometimes necessary to select and measure a lower amplitude signal among multiple signals. To meet this need, the counter provides a center frequency mode in Band 3. Figure 3-7 shows an example of the center frequency feature. If the signals shown in the figure are applied to Band 3, the counter would, in normal operation, select the signal at 6.2 GHz, since it is the highest amplitude signal. The center frequency mode makes it possible to select any of the signals shown. For example, to select the signal at 6.3 GHz, a center frequency of 6.3 GHz is entered. This limits the frequency search to a narrow range centered at 6.3 GHz, and prevents the counter from selecting either of the other two higher amplitude signals.

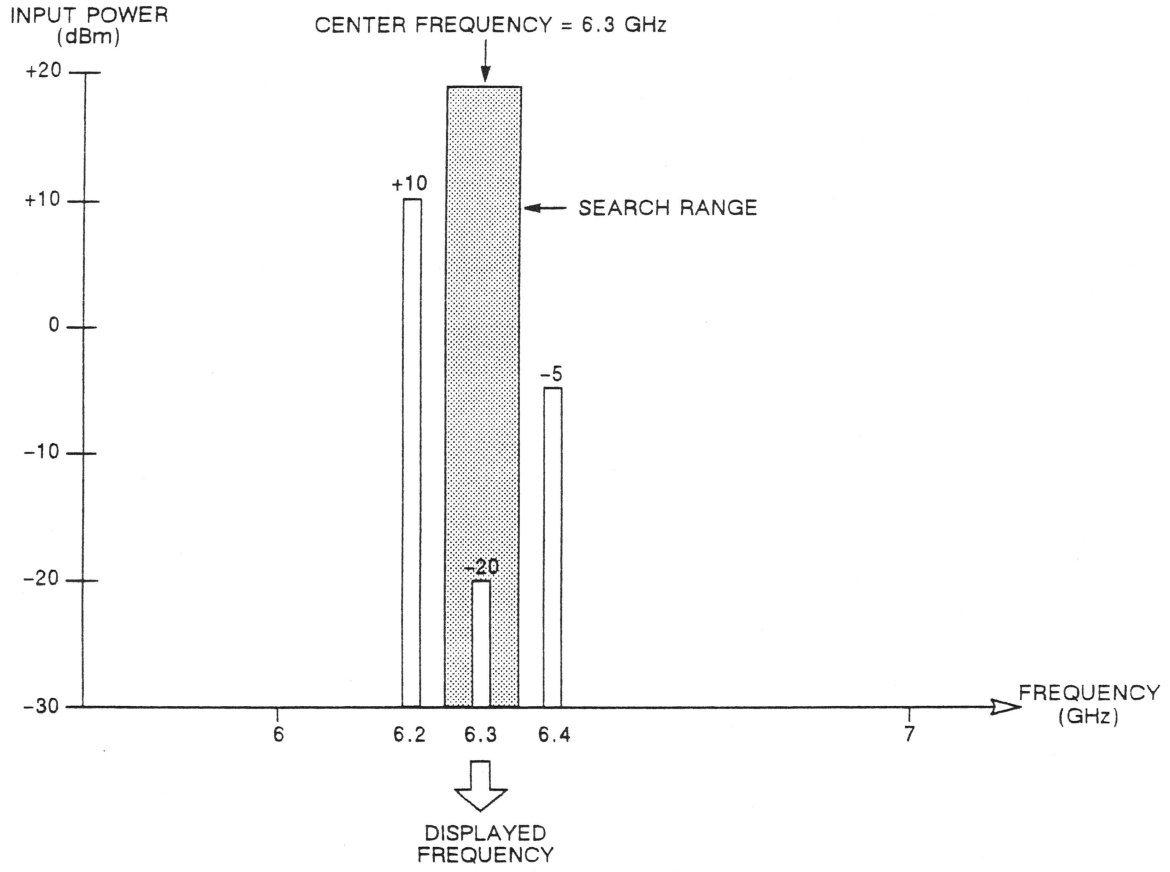



**Figure 3-7. Center Frequency.**

## COUNTER ACCURACY

When making any type of measurement, some degree of measurement error exists. In EIP CW counters, measurement error is a result of a combination of time base error and gate phasing error (±1 count).

The measurement error is specified as:

Measurement error = time base error ±1 count (gate phasing error)

A frequency error in the time base oscillator results in a proportional error in the frequency measurement. An example would be the aging rate of the internal time base, specified to be less than $1 \times 10^{-7}$ parts per month. This means that if the oscillator is set precisely on frequency at the

beginning of a month, it could be as much as 1 Hz off at the month's end. On a frequency measurement of 18 GHz, a 1 Hz error in the 10 MHz time base would cause a measurement error of 1.8 kHz.

Time base error is caused by the following factors:

- temperature stability
- line variation
- aging rate
- short-term stability

Temperature stability refers to variation in output frequency of an oscillator caused by changes in temperature. The counter's internal time base is a temperature compensated crystal oscillator (TCXO) with components that compensate for temperature-related frequency drift.

Variations in the line voltage applied to the counter cause variations in the oscillator frequency. The counter provides regulation to improve line stability and minimize time base frequency variance.

Aging rate is the long-term frequency drift that occurs in an oscillator, and is a function of the inherent characteristics of the crystal.

Short-term stability is the ongoing random frequency fluctuations that occur in oscillator output. The primary cause of short-term frequency fluctuation is circuit noise.

Gate phasing error, the second source of measurement error, is caused by the relative timing of the gate and the arrival of the signal to be counted. This results in an uncertainty of ±1 count in the least significant digit of the measurement. For example, if the counter resolution is set to 1 kHz, then the potential error on each gate is ±1 kHz. Figure 3-8 illustrates gate phasing error. The incoming signal, after passing through the signal conditioner, appears at the main gate as a pulse train. Gate B, though the same width as Gate A, counts three events (pulses corresponding to signal zero-crossings) while Gate A counts only 2.

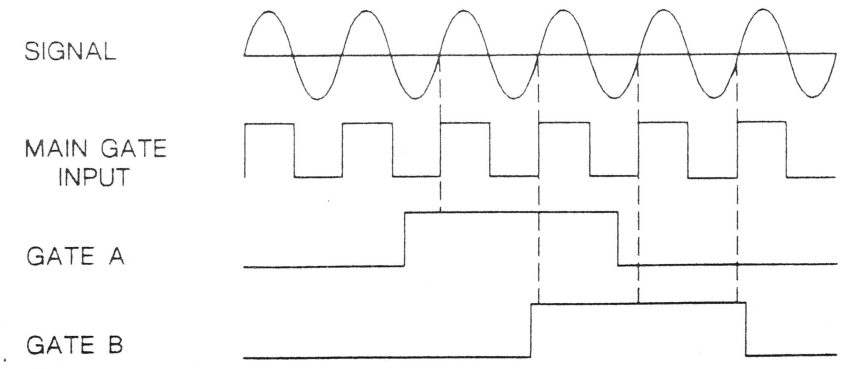



**Figure 3-8. Gate Phasing Error.**

## TECHNIQUES FOR IMPROVING ACCURACY

In most cases, the specified accuracy of the EIP 625A counter will be more than sufficient to meet measurement requirements. Greater accuracy, if required, can be achieved by minimizing error in the time base, since this is the primary source of measurement error.

Temperature effects on the time base are minimized by calibrating the time base at the temperature at which the counter will be used, using a time base of higher accuracy. Long-term frequency drift can be minimized by frequent calibration of the time base. Finally, an external time base with a higher degree of accuracy can be used, such as a 10 MHz oven oscillator, or a rubidium or cesium beam frequency standard.

## CALCULATING MEASUREMENT ERROR

Following is a sample calculation for determining the measurement error of the counter, based on the time base aging rate.

Given: Aging rate: $1 \times 10^{-7}$/month
Calibration interval: 6 months
Frequency: 20 GHz

Calculation: Error $= \pm$(aging rate x cal. interval x frequency)

$$= \pm\left(\frac{1 \times 10^{-7}}{\text{mo.}} \times 6 \text{ mo.} \times 2 \times 10^{10} \text{ Hz}\right)$$

$$= \pm(6 \times 10^{-7} \times 2 \times 10^{10} \text{ Hz})$$

$$= \pm(12 \times 10^{3} \text{ Hz})$$

$$= \pm 12 \text{ kHz}$$

Counter measurement, after the recommended six month calibration interval, could have an error of $\pm$12 kHz in measuring a 20 GHz signal.

This example is for illustrative purposes only. Actual calculation of measurement error must include the other sources of time base error, as well as gate phasing error.

## SPECIAL FUNCTIONS

The special functions of the EIP 625A counter can be divided into three categories:

1. Counter operation verification
2. Calibration/troubleshooting aids
3. Counter capability enhancements

### ONE-SHOT OR CONTINUOUS ACTION SPECIAL FUNCTIONS

Each special function is labeled as being either a one-shot or a continuous action function:

- One-shot functions – automatically revert the counter to its normal operation after a specific action has been taken.

- One-shot/CLEAR DISPLAY functions - after a specific action has been taken, require a press of the CLEAR DISPLAY key to return the counter to normal operation.
- Continuous action functions - stop all normal operations of the counter and cause it to stay in the special function mode until the user terminates the function. Most continuous action functions can be terminated by pressing the CLEAR DISPLAY key or entering any function command through the GPIB interface. After the special function is terminated, the function corresponding to the key pressed or the command entered will be serviced and a reset will be generated. Exceptions to the above termination sequence are stated in the individual special function descriptions.

### SPECIAL FUNCTION (SPC) INDICATOR ON OR OFF

The SPC ON/OFF notation at the end of a special function description indicates whether the SPC status indicator on the front panel is on or off upon exiting this function. The SPC status indicator is also accessible via the GPIB.

### OPERATION VERIFICATION FUNCTIONS

SPECIAL FUNCTION 01: 100 MHz Self-Test

This function verifies operation of the count chain, gate generator, and VCO. The display shows 100 MHz ±1 count. These results are output to the GPIB interface when frequency readings are requested.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 02: Light Display Segments Test

This function verifies that all digit segments and annunciator LEDs are operational. When this function is activated, all digit segments and all annunciators are turned on.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 03: Scan Display Segments Test

Each segment in all the digits and the bank of annunciators is turned on sequentially by this function to test the display segment drivers. The scan rate is determined by the setting of the SAMPLE RATE up and down controls. For manual control, activate sample rate hold, and press the "." key to activate a single segment.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 04: Scan Display Digits Test

Each digit and each bank of annunciators is turned on sequentially by this function to check the display digit driver. The scan rate is determined by the setting of the SAMPLE RATE up and down controls. For manual control, activate sample rate hold, and press the "." key to activate a single digit or annunciator.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 05: Keyboard Test

This function verifies the operation of the keyboard. When this function is activated, the counter stops normal operations, and the display shows the key code of the last key pressed. (See table.) When a new key is pressed, the display is updated to show the code of the new key. The CLEAR DISPLAY key will not return a key code, but will instead return the counter to normal operation. When the GPIB controller requests a key code, the code of the last key pressed is output. If the controller requests a

key code, the counter outputs to the GPIB interface the code of the last key pressed even if Special Function 05 is not activated. If the counter is in local, this function must be terminated by the CLEAR DISPLAY key. If it is in remote, this function can be terminated by any device-dependent command.

CONTINUOUS SPC INDICATOR: ON

| Key | Code |
|---|---|
| SPECIAL FUNC | 35 |
| BAND | 36 |
| 0/RESET LOCAL | 31 |
| 7/SAMPLE RATE up | 12 |
| 4/FREQ offset | 22 |
| 1 | 32 |
| 8/SAMPLE RATE hold | 13 |
| 5/CENTER FREQ | 23 |
| 2 | 33 |
| 9/SAMPLE RATE down | 14 |
| 6/FREQ mult | 24 |
| 3 | 34 |
| GHz | 15 |
| MHz | 25 |
| "." (decimal or trigger) | 21 |
| CLEAR DATA | 16 |
| CLEAR DISPLAY | exits test |
| RESOL | 11 |

SPECIAL FUNCTION 06: PROM Check Sum Test

This function generates the check sum for the PROM in the counter and compares it with the check sum stored in the firmware. If the check sum generated is correct, the counter displays the word "PASSEd" on the front panel. If the check sum is incorrect, an error message is output to the display. At the same time, the ERROR CONDITION status bit in the GPIB serial poll status byte is set. During check sum generation, "SPECIAL 06" is displayed.

ONE-SHOT/CLEAR DISPLAY SPC INDICATOR:ON

SPECIAL FUNCTION 07: Display Counter Model Number and GPIB Address

This function displays the counter's model number and GPIB address. No reset is generated.

ONE-SHOT/CLEAR DISPLAY SPC INDICATOR:ON

SPECIAL FUNCTION 08: External Time Base Select

Selecting this function causes the counter to accept an external time base input. When this function is enabled, the EXT indicator on the front panel comes on.

ONE-SHOT SPC INDICATOR:OFF

SPECIAL FUNCTION 09: Internal Time Base Select

Selecting this function causes the counter to use its internal 10 MHz time base.

ONE-SHOT SPC INDICATOR:OFF

## CALIBRATION/TROUBLESHOOTING AIDS

Special Functions numbered 20 through 47 aid the user in calibrating and/or troubleshooting the counter.

SPECIAL FUNCTION 20: Band 3 Detected RF Level

This function displays the relative power level of the input signal. It verifies coarse calibration of the Band 3 YIG DAC offset and YIG DAC slope adjustments. When this function is activated, the counter waits for the user to enter the new YIG calibration frequency. The previously entered frequency and "Fr" are displayed. The special function stops in this state until the user enters a new frequency.

After the number has been entered, the YIG DAC is set to the entered frequency. The display shows "CAL DAC" plus a number from 0 to 8 corresponding to the information on the Band 3 power discrimination circuitry. To activate this function via the GPIB, Y3FREQ must be specified, and then Special Function 20 must be called. The counter will output the power discrimination circuitry information when requested by the GPIB to output LEVEL.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 40: Sweep YIG DAC

When this function is activated, the counter waits for the user to enter the start frequency of the YIG sweep. The previously entered start frequency and "F1" are displayed. The special function stops in this state until the user enters a new start frequency.

After the start frequency is entered, the counter waits for the user to enter the stop frequency of the YIG sweep. The previously entered stop frequency and "F2" are displayed. The special function stops in this state until the user enters a new stop frequency.

When both the start and stop frequencies have been entered, the display reverts to "SPECIAL 40." The YIG DAC sweeps continuously from F1 to F2 in 2 MHz steps until the function is terminated. If F1 and F2 are equal, the YIG DAC is set to that particular frequency. The sweep rate is controlled by the SAMPLE RATE up and down controls, and maximum sweep rate is obtained by disabling the sample rate (Special Function 63) before calling this function. For manual control, activate sample rate hold, and press the "." key to generate a single sweep.

To activate this function via the GPIB, start and stop frequencies Y1FREQ and Y2FREQ must first be specified (where Y1FREQ and Y2FREQ correspond to F1 and F2 respectively), then Special Function 40 must be called. If the start or stop frequency required is different from that previously specified in Y1FREQ or Y2FREQ, the number in that frequency register must be updated before Special Function 40 is called.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 41: Sweep VCO with VCO Power Amplifier On

After this function is activated, the counter waits for the user to enter the start frequency of the VCO sweep. The previously entered start frequency and "F1" are displayed. The special function stops in this state until the user enters a new start frequency.

After the start frequency is entered, the counter waits for the user to enter the stop frequency of the VCO sweep. The previously entered stop frequency and "F2" are displayed. The special function stops in this state until the user enters a new stop frequency.

When both the start and stop frequencies have been entered, the display reverts to "SPECIAL 41." The VCO is swept continuously from F1 to F2 in 100 kHz steps until the function is terminated. If F1 and F2 are equal, the VCO is set to that particular frequency. The VCO power amplifier is turned on during this function.The sweep rate is controlled by the setting of the SAMPLE RATE up and down controls. Maximum sweep rate is obtained by disabling the sample rate (Special Function 63) before calling this function. For manual control, activate sample rate hold, and press the "." key to generate a single sweep.

To activate this function via the GPIB, the user instructs the controller to output SPECIAL 41. The start and stop frequencies used are the frequencies specified in the GPIB commands V1FREQ and V2FREQ (where V1FREQ and V2FREQ correspond to F1 and F2, respectively). If the start or stop frequency required is different from that specified in V1FREQ or V2FREQ, the number in that frequency register must be updated before SPECIAL 41 is activated.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 42: Sweep VCO with VCO Power Amplifier Off

After this function is activated, the counter waits for the user to enter the start frequency of the VCO sweep. The previously entered start frequency and "F1" are displayed. The special function stops in this state until the user enters a new start frequency.

After the start frequency is entered, the counter waits for the user to enter the stop frequency of the VCO sweep. The previously entered stop frequency and "F2" are displayed. The special function stops in this state until the user enters a new stop frequency.

When both the start and stop frequencies have been entered, the display reverts to "SPECIAL 42." The VCO is swept continuously from F1 to F2 in 100 kHz steps until the function is terminated. If F1 and F2 are equal, the VCO will be set to that particular frequency. The VCO power amplifier is turned off during this function.The sweep rate is controlled by the SAMPLE RATE up and down controls. Maximum sweep rate is obtained by disabling the sample rate (Special Function 63) before calling this function. For manual control, activate sample rate hold, and press the "." key to generate a single sweep.

To activate this function via the GPIB, the user instructs the controller to output SPECIAL 42. The start and stop frequencies used are the frequencies specified in the GPIB commands V1FREQ and V2FREQ (where V1FREQ and V2FREQ correspond to F1 and F2, respectively). If the start or stop frequency required is different from that specified in V1FREQ or V2FREQ, the number in that frequency register must be updated before SPECIAL 42 is activated.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 44: Disable Normal Operations

This function prevents the counter from performing the normal converter lock and measurement cycles. It freezes the counter in the state it was in when the function was activated and displays PAUSE. Special Function 44 remains activated until terminated by Special Function 45.

CONTINUOUS SPC INDICATOR:ON

SPECIAL FUNCTION 45: Enable Normal Operations

This function returns the counter from Special Function 44 to normal operation. A reset is generated and the STOP ON/OFF status bit is cleared when this function is activated.

CONTINUOUS SPC INDICATOR:OFF

SPECIAL FUNCTION 46: Display and/or Alter Memory

## CAUTION

**Care must be used when operating Special Function 46. Although the counter cannot be damaged by this function, stored calibration data can be changed. For this reason, access to this function is blocked by an internal memory protect switch. Attempting to access this function with the memory protect switch in the protect position will cause the counter to display "ERROR 53."**

### NOTE

See Service Manual for instructions on unprotecting memory.

This function provides the user with a means to display and/or alter any memory location. The counter continues its normal operations when it is performing this function unless Special Function 44 has previously been activated.

After this function is activated, the counter waits for a memory address to be entered. During this time, "Addr----" is displayed. As the address is entered, the hexadecimal digits keyed will replace each blank (-) sequentially. After the memory address is entered, the content of that memory location is exhibited in the last three digits of the display.

At this point the user can do one of the following:

1. Exit the function by issuing a CLEAR DISPLAY command.
2. Alter the content of the memory location by entering a two-digit hexadecimal number.
3. Enter another memory address by first issuing an ADDRESS command (pressing the CLEAR DATA key).

If the content of a memory is altered, the new content of that memory location is displayed. If the ADDRESS command is issued, the display will change to show "Addr----", prompting for the input of hexadecimal digits to replace the blanks in the display and complete the memory address. The content of the entered memory address will then be displayed.

In the local mode, the keys on the keyboard take on different meanings after Special Function 46 is activated. Following are the definitions of the keys when the counter is in this function:

- All number keys remain number keys
- GHz key = hexadecimal digit A
- MHz key = hexadecimal digit B
- "." (decimal or trigger) key = hexadecimal digit C
- "±" key = hexadecimal digit D
- SPECIAL FUNC key = hexadecimal digit E

- BAND key = hexadecimal digit F
- CLEAR DATA key = ADDRESS command
- CLEAR DISPLAY key remains the same

In the remote mode, a memory content can be interrogated by using the OUTPUT MEMORY command. When the counter is addressed to talk, the last memory address accessed will be output. A memory location can be accessed using the MEMORY OHHHH command (where each H represents a hexadecimal digit). The content of a memory location can be altered using the MEMORY OHHHH OHH command. In the remote mode, Special Function 46 need not be activated when accessing and altering memory locations. Those operations can be done by the controller in the background.

CONTINUOUS SPC INDICATOR:ON

---

SPECIAL FUNCTION 47: Count Chain Test

---

This function provides the user with the means to measure the frequency of the signal present at the input of the count chain assembly without having the counter converter locked on the signal.

When this function is activated, the counter stops the normal converter lock and measurement cycles. The VCO, YIG, and all microprocessor-controlled hardware switches will be left at the state they were in when the function was activated. The counter then starts measuring the frequency of the signal present at the the input to the count chain assembly. The measurement results are displayed on the front panel. The result is also output to the GPIB interface if frequency readings are requested. This function does not check periodically for the presence of a signal as in the normal operation of the counter.

CONTINUOUS SPC INDICATOR:ON

---

## CAPABILITY ENHANCEMENT FUNCTIONS

Special Functions 61 through 91 provide users sophisticated additional functions not required in normal operation.

---

SPECIAL FUNCTION 61: Disable Input Signal Tracking

---

This function stops the counter from tracking the input signal after every measurement cycle, thus shortening the measurement cycle time. This function is canceled by Special Function 62.

ONE-SHOT SPC INDICATOR:ON

---

SPECIAL FUNCTION 62: Enable Input Signal Tracking

---

This function cancels Special Function 61.

ONE-SHOT SPC INDICATOR:OFF

---

SPECIAL FUNCTION 63: Disable Sample Rate Control

---

This function causes the counter to ignore the local and the remote sample rate controls. The counter starts a new measurement cycle immediately upon the termination of the previous one, thus shortening the measurement cycle time. This function is canceled by Special Function 64.

ONE-SHOT SPC INDICATOR:ON

SPECIAL FUNCTION 64: Enable Sample Rate Control

This function cancels Special Function 63 and sets the sample rate to maximum.

ONE-SHOT SPC INDICATOR:OFF

SPECIAL FUNCTION 65: Disable Measurement Display

This function inhibits the output of the measurement results to the front panel display which, alternatively, displays a row of dots. When the user enters parameters through the keyboard,the display responds normally. This function shortens the measurement cycle time and provides security in systems used with classified frequencies. This function is canceled by Special Function 66.

ONE-SHOT SPC INDICATOR:ON

SPECIAL FUNCTION 66: Enable Measurement Display

This function cancels Special Function 65. When this function is activated, the display will indicate the most recent measurement results.

ONE-SHOT SPC INDICATOR:OFF

SPECIAL FUNCTION 72: Store Counter Setup and/or Default Values

This function serves two purposes. Its primary use is to store the current counter setup in the storage register specified. When activated via the front panel, the counter requests the user to enter the register number by displaying "REG-." The counter remains in this state until entry of a register number between 0 and 9, inclusive. After the register number is entered, the function proceeds to store the current counter setup in the register specified. During this time, "REG N" is displayed on the front panel, where N is the number of the specified register. To store the counter setup using GPIB, issue the command STORE N, where N is the register number.

This function can also be used to customize the default values of the counter, which determine the state of the counter at turn-on. This is accomplished, via the keyboard, by setting the instrument up in the desired turn-on condition and then storing that state in register 0, using Special Function 72. The information stored in register 0 determines the power-on state of the counter. To accomplish this using GPIB, the command STORE 0 is used. To clear the instrument and return it to the factory-set default values, select Special Function 72 and press the CLEAR DATA key. To return the counter to the factory-set state using GPIB, jssue the command STORE DEFAULT.

ONE-SHOT SPC INDICATOR:OFF

SPECIAL FUNCTION 73: Recall Counter Setup

This function recalls the counter setup stored in the storage register specified. When this function is activated, the counter requests entry of the register number by displaying "REG-." The counter remains in this state until entry of a number between 0 and 9, inclusive. After the register number is entered, the function proceeds to set up the counter in agreement with the information stored in the register specified. During this time, "REG N" will be displayed on the front panel, where N is the register number specified. When the counter setup is completed, a reset is generated. To recall a stored counter setup using GPIB, issue the command FETCH N, where N is the register number. (NOTE: Unless new setup values (different from the factory-set values) have been stored in register 0, recalling this register will generate Error 06. Press the CLEAR DISPLAY key, or, using GPIB, issue the CLEARDISPLAY command to return the counter to normal operation.)

ONE-SHOT SPC INDICATOR:OFF

SPECIAL FUNCTION 74: Relative Frequency Readings

When this function is activated, the counter assigns a negative value to the last input frequency reading and enters it into the frequency offset register (overwriting any previously entered frequency offset). This is the actual frequency of the input signal, not the frequency displayed on the front panel. The counter displays the sum between the current frequency and the offset, subject to any other functions activated. It will continue until the FREQ offset and CLEAR DATA keys are pressed. The OFS indicator is lit while this function is active.

CONTINUOUS SPC INDICATOR:OFF

SPECIAL FUNCTION 75: Display IF Frequency Readings

When this function is activated, the counter assigns a negative value to the local oscillator (LO) frequency and enters it into the frequency offset register (overwriting any previously entered frequency offset). The counter subtracts the LO frequency from the input frequency and displays the resulting IF. It continues to do so until the FREQ offset and CLEAR DATA keys are pressed. The OFS LED is turned on.

CONTINUOUS SPC INDICATOR:OFF

SPECIAL FUNCTION 76: EEPROM Test

## CAUTION

**Care must be used when operating Special Function 76. Although the counter cannot be damaged by this function, if execution of this function is interrupted prior to completion, a loss of the data contained in the EEPROM will occur. For this reason, access to this function is blocked by an internal memory protect switch. Attempting to access this function with the memory protect switch in the protect position will cause the counter to display "ERROR 53."**

This function allows the user to test the EEPROM.

This function performs write and read tests on each location on the EEPROM. If any one location on the EEPROM fails the write and read tests, "ERROR 94" is displayed. If all memory locations pass the tests, "PASSEd" is displayed.

This function requires approximately two minutes to complete. During those two minutes, the counter will not respond to any entry from the keyboard.

ONE-SHOT SPC INDICATOR:ON

SPECIAL FUNCTION 90: Display and/or Alter GPIB Address

The counter displays the current GPIB address. The function is terminated by pressing either the CLEAR DISPLAY or CLEAR DATA key.

The GPIB address is changed by entering a two-digit number between 01 and 99 inclusive. The function is terminated and the display returned to displaying measurement results after the second digit key is released.

ONE-SHOT/CLEAR DISPLAY SPC INDICATOR:ON

SPECIAL FUNCTION 91: YIG DAC Automatic Calibration

This function calibrates the Band 3 input filter. Refer to the 625A Service Manual for complete information.

## ERROR MESSAGES

Error messages are displayed in the following format: ERROR XX, where XX is the two-digit error code.

01 Invalid key sequence
04 Center frequency entry only in Band 3
05 Center frequency entry outside band range
06 No valid data in storage registers for recall feature
07 Converter unable to lock on signal during special
09 Invalid register entry
10 Invalid band entry
12 Invalid resolution entry
13 Invalid special function entry
15 Invalid multiplier entry
16 Invalid frequency offset entry
17 Invalid center frequency entry
21 Invalid sample rate entry
22 Invalid SRQ number entry
23 Invalid GPIB address
24 Invalid VCO frequency 1 entry
25 Invalid VCO frequency 2 entry
26 Invalid YIG frequency 1 entry
27 Invalid YIG frequency 2 entry
28 Invalid YIG DAC frequency entry
29 Frequency overflow due to multiplier
31 GPIB input message too long
32 GPIB message starts with a number
34 Unrecognized GPIB command
36 Missing space
37 Wrong mode argument
40 Non-numeric parameter value
41 Wrong frequency terminator
43 Wrong output argument
44 Numeric argument syntax error
45 Numeric mantissa has too many digits
46 Numeric exponent has too many digits
47 HEX data should be preceded with a zero
48 No HEX memory address specified
49 Invalid HEX data entry
50 Invalid HEX address entry
52 Invalid entry
53 Access to this function blocked by memory protect switch
60 RAM fault
61 ROM check sum error: ADDR 4000 to 7FFF
62 ROM check sum error: ADDR 8000 to BFFF
63 Activate SPC 72 and 73 through store and fetch
90 No key release detected
91 Option not installed
94 Nonvolatile memory failure
99 No IF detected

# SECTION 4
# PROGRAMMING

## REMOTE PROGRAMMING

### GENERAL PURPOSE INTERFACE BUS

The GPIB interface in the 625A counter conforms to the IEEE Code and Format conventions and the IEEE 488 - 1978 Standards. Using the GPIB interface, the counter can respond to remote control instructions and can output measurement results. At the simplest level, the counter can output data to other devices, such as a printer. In more sophisticated systems, an instrument controller or computer can program the counter remotely, trigger measurements, and read results. A quick reference list of GPIB commands is located at the end of this section.

### GPIB FUNCTIONS IMPLEMENTED

The following GPIB interface function subsets are implemented:

| Interface Function | Subset | Description |
|---|---|---|
| SOURCE HANDSHAKE | SH1 | Complete capability |
| ACCEPTOR HANDSHAKE | AH1 | Complete capability |
| TALKER | T5 | Basic talker, serial poll, talk only mode, unaddress if MLA |
| LISTENER | L4 | Basic listener, unaddress if MTA |
| SERVICE REQUEST | SR1 | Complete capability |
| REMOTE/LOCAL | RL1 | Complete capability |
| DEVICE CLEAR | DC1 | Complete capability |
| DEVICE TRIGGER | DT1 | Complete capability |

For remote operation, the 625A counter provides the following capabilities:

- Acceptance of device-dependent messages to set the instrument measurement mode and parameters. The input buffer can store up to 256 characters from the bus. Execution of the device-dependent messages starts after the first message separator is accepted. Input of more characters will interrupt the execution so that the additional characters are accepted and stored for fast bus response (unless buffer is full).
- Output of measurement results, any parameter value, or instrument mode on demand from the system controller.
- Configuration of the output format in several ways to accommodate different system controllers and speed requirements.
- Implementation of device clear and selected device clear functions to configure the instrument to the power-up state. See page 4-9 for the counter's power-up configuration.
- Implementation of group execute trigger (GET) message to start a new measurement cycle.
- Implementation of serial poll functions to allow the system controller to get a status byte from the instrument that gives status information for various functions. The instrument can also be instructed to interrupt (SRQ) the controller on any ORed or ANDed combination of the status events.
- Implementation of remote/local transitions. When the counter is in remote, all front and rear panel keys and switches are disabled (except the POWER switch). Remote/local transitions will not change any instrument configuration (except the sample rate settings, which will override in a remote-to-local transition). When the counter changes from local to remote functioning, or

vice-versa, all stored information is retained. The counter will operate in the same state as before the change. The exception is that, when the counter is performing a special function during a transition, the special function will be terminated.

- Implementation of local lockout, with the RESET/LOCAL key disabled accordingly. When the counter is in remote, and local lockout is not active, the RESET/LOCAL key on the front panel acts as the return-to-local key.
- Front panel annunciator to indicate remote (RMT) operation.
- Recognition of all three bus terminators: CR LF (carriage return line feed), NL (null), and EOI (end or identify).
- Implementation of talk-only modes for no-controller applications.

## DEVICE-DEPENDENT MESSAGES (LISTENER FEATURES)

A device-dependent message generally consists of reserved words and numbers. The message structure depends on the type of message, and can be:

- Header only
- Header and argument
- Header and argument and terminator

Where the header is a reserved word, the argument is a number or a reserved word, and the terminator is a reserved word.

Messages can be linked with a comma (,) or semicolon (;) as separators. A message chain can be terminated with CR LF or NL or EOI. Any device-reserved word will be recognized by at least the first two characters of the word, with the exception of RESET which requires entry of the first four letters (RESE). The first two characters of each command are printed in **large boldface** type in the following command lists to promote user familiarity with the shortened form of the command. Spelling of more characters (up to the full word) is optional for user program readability.

Example: INITIALIZE
INITIAL
INIT
IN
are all recognized equivalently

A <number> can be sent in any of the defined IEEE formats (NR1, NR2, NR3).

Example: 12000
12000.00
001.2e4
.12000E+5
are all recognized equivalently

NOTE

The reserved word DEFAULT can replace a numeric argument for default value assignment. The terminator in the parameter messages group is optional, and defaults to Hz or s.

A command message having a header and argument (e.g., HOLD ON) must have a space separating the header and argument. However, this is optional if the second word is a number (OFFSET4.3e9 and OFFSET 4.3E9 are recognized equivalently). Additional spaces in front of words, between words, or after a message are optional, and will be ignored. Nulls and CRs are ignored anywhere. Both upper and lower case characters are acceptable.

Control, mode, and parameters messages are all used with the controller in the listener mode to enter instructions and data.

**Control Messages**

| Header | Argument | Terminator | Description |
|---|---|---|---|
| **CL**EARDISPLAY | None | None | Returns the display to normal measurement results display, and clears errors (equivalent to front panel CLEAR DISPLAY key). |
| **IN**ITIALIZE | " | " | Reconfigures the instrument to power-up state. All parameters are set to default values. |
| **RESE**T | " | " | Resets counter to initiate a new signal acquisition cycle (equivalent to front panel key). |
| **TR**IGGER | " | " | Triggers a new measurement cycle (equivalent to front panel "." key). |

**Mode Messages**

| Header | Argument | Terminator | Description |
|---|---|---|---|
| **DY**NAMIC | ON or OFF | None | Suppresses blanks when the counter is configured in talker mode for faster free-field data transfer. |
| **EX**TERNAL | " | " | Controls the INT/EXT time base reference. (Special Function 08 can also be used to select the external time base.) |
| **HE**ADER | " | " | Adds an alpha header and terminator for talker. |
| **HO**LD | " | " | Holds the last result if ON (equivalent to front panel HOLD). |
| **SC**IENTIFIC | " | " | Selects scientific notation for talker. |
| **SE**PARATE | " | " | Replaces the commas with CR LF between multinumber results. |

**NOTE**

In the local mode, SAMPLE RATE and HOLD are controlled via the front panel controls, but in remote the front panel controls are not active. In the remote mode, both SAMPLE RATE and HOLD are under software control. Refer to GPIB SAMPLERATE and HOLD commands.

**Parameter Messages**

| Header | Argument | Terminator | Description |
|---|---|---|---|
| **AS**RQMASK | <number> | None | Selects the ANDed combination of status events to cause a service request. |
| **BA**ND | " | " | Selects a specific band (1 to 3) or DEFAULT. |
| **CE**NTERFREQ | " | (Hz/kHz/MHz/GHz) | Sets a center frequency value and mode. |

Parameter Messages (Continued)

| Header | Argument | Terminator | Description |
|---|---|---|---|
| FETCH | " | None | Recalls counter setup stored in specified storage register (0 to 9) (see Special Function 73). |
| MEMORY | <hex_adrs> | <hex_data> | Accesses a memory location and alters it (altering is optional). |
| MEMORY | INCREMENT | " | Accesses the next location and alters it (altering is optional). |
| MEMORY | DECREMENT | " | Accesses the previous location and alters it (altering is optional). |
| MULTIPLIER | <number> | None | Inputs a multiplier value (0 to 99). |
| OFFSETFREQ | " | (Hz/kHz/MHz/GHz) | Sets a frequency offset value (1 kHz to 99.9 GHz). |
| RESOLUTION | " | None | Sets the frequency measurement resolution (.1 in Band 1 only and 0 to 9). |
| SAMPLERATE | " | (s/ms) | Sets a delay between measurement cycles (0 to 100 sec, 10 ms resolution). |
| SPECIAL | " | None | Activates a specific special function (01 to 99). |
| SRQMASK | " | " | Selects the ORed combination of status events to cause a service request. |
| STORE | " | " | Stores current counter setup in specified storage register (0 to 9) (see Special Function 72). |
| V1FREQ | " | (Hz/kHz/MHz/GHz) | Sets a start frequency for VCO sweep (see Special Functions 41, 42). |
| V2FREQ | " | " | Sets a stop frequency for VCO sweep (see Special Functions 41, 42). |
| Y1FREQ | " | " | Sets a start frequency for YIG sweep (see Special Function 40). |
| Y2FREQ | " | " | Sets a stop frequency for YIG sweep (see Special Function 40). |
| Y3FREQ | " | " | Sets YIG frequency (see Special Function 20). |

### Output Control Messages

These commands are used with the controller in the talker mode to request the output of data.

| Command | Description |
|---|---|
| OUTPUT BAND | Outputs the number of the current band. |
| OUTPUT CENTERFREQ | Outputs the center frequency last specified. |
| OUTPUT DATE | Outputs a 25-character string that shows the EIP part number, revision level, and date of the instrument firmware contained in the PROM on the microprocessor assembly. |

Output Control Messages (Continued)

| Command | Description |
|---|---|
| **OU**TPUT **ER**RORNUMBER | Outputs the number of the last error (see listing of error numbers on page 3-20). |
| **OU**TPUT **ID**ENTIFICATION | Outputs "EIP625A GPIB dd", where dd is the GPIB address. |
| **OU**TPUT **KE**YCODE | Outputs the code of the last key pressed. |
| **OU**TPUT **LE**VEL | Outputs a number between 0 and 8 corresponding to the signal level applied to Band 3 (see Special Function 20). |
| **OU**TPUT **ME**MORY | Outputs the contents of the memory in the last accessed location. |
| **OU**TPUT **MU**LTIPLIER | Outputs the current multiplier value. |
| **OU**TPUT **OF**FSETFREQ | Outputs the current offset frequency. |
| **OU**TPUT **RE**SOLUTION | Outputs the current frequency measurement resolution. |
| **OU**TPUT **SA**MPLERATE | Outputs the current delay time between measurement values. |
| **OU**TPUT **SE**TUP | Outputs a 106-character string that describes the current setup (see below). |
| **OU**TPUT **SR**QMASK | Outputs the combination of status events required to cause a service request (see page 4-8). |
| **OU**TPUT **V1**FREQ | Outputs the current start frequency for VCO sweep (see Special Functions 41 and 42). |
| **OU**TPUT **V2**FREQ | Outputs the current stop frequency for VCO sweep (see Special Functions 41 and 42). |
| **OU**TPUT **Y1**FREQ | Outputs the current start frequency for YIG sweep (see Special Function 40). |
| **OU**TPUT **Y2**FREQ | Outputs the current stop frequency for YIG sweep (see Special Function 40). |
| **OU**TPUT **Y3**FREQ | Outputs the current YIG frequency (see Special Function 20). |

### Output Setup Command

The output setup command causes the counter to output a 106-character string that corresponds to the current setup of the instrument. The following sample program, for the HP Model 320 controller, can be used to obtain the default setup string:

```
10   DIM A$[110]                    ! Dimension a variable to hold the string
20   OUTPUT 718;"OUTPUT SETUP"      ! send command to counter
30   ENTER 718;A$                   ! get output from counter
40   DISP A$                        ! display output on HP Model 320
```

Setup string: BA3,RE00,MU01,OF+000000000KH,LO000800MH,HI020500MH,
CE000000MH,SA000000MS,SR000,SP62,SP64,SP66,SP45,HO0,EX0

The following list can be used to decode the returned setup string. The information contained in the parentheses will change depending on the current setup of the instrument.

BA3: BAND (3)
RE00: RESOLUTION (0)

| | |
|---|---|
| MU01: | MULTIPLIER (1) |
| OF+000000000KH: | FREQUENCY OFFSET (0) |
| LO000800MH: | LOW LIMIT = (800) MHz |
| HI020500MH: | HIGH LIMIT = (20.5) GHz |
| CE000000MH: | CENTER FREQUENCY (0) NOT ACTIVE |
| SA000000MS: | SAMPLE RATE = (0) ms (Maximum sample rate) |
| SR000: | SERVICE REQUEST MASK OFF |
| SP62: | SPECIAL FUNCTION (62) ACTIVE |
| SP64: | SPECIAL FUNCTION (64) ACTIVE |
| SP66: | SPECIAL FUNCTION (66) ACTIVE |
| SP45: | SPECIAL FUNCTION (45) ACTIVE |
| HO0: | HOLD (0) OFF |
| EX0: | TIME BASE (0) INTERNAL |

### Output and Format Example

The following program illustrates how controllers function with the counter and how different kinds of controllers give instructions. These programs set the counter up in a sample configuration and program it to make a series of measurements of a 12.5 GHz signal. The talk and listen address of the counter is assumed to be 18.

- Hewlett Packard Model 320

```
10 DIM A$[18]
20 OUTPUT 718;"IN"
30 WAIT 4000
40 OUTPUT 718;"BAND 3"
50 OUTPUT 718;"RE 4"
60 WAIT 1000
70 ENTER 718;A$
80 DISP A$
90 END
```

This Model 320 program initiates the counter, selects Band 3, provides a resolution value, and instructs it to output the frequency to the controller display. The controller display would appear something like this:

12500000000

## OUTPUT MESSAGES (TALKER FEATURES)

After receiving a talk address, the GPIB will output the current configuration or any parameter value or measurement result, in response to the appropriate output control message. After power-up or device-clear, the controller outputs the displayed measurement results (as it does after the OUTPUT DEFAULT command).

The format of each output message can be controlled by the following features:

- SCIENTIFIC - provides exponential notation with engineering exponents when SCIENTIFIC is ON. Default is OFF.
- DYNAMIC - suppresses blanks and trailing zeros for faster data transfer when DYNAMIC is ON. Default is OFF.
- HEADER - provides an alpha header and terminator around each numeric data item for clarity, (useful for printers) when HEADER is ON. Default is OFF.

**NOTE**

Terminator takes over the exponential role if both SCIENTIFIC and HEADER are ON.

- Default – the data output format when SCIENTIFIC, DYNAMIC, and HEADER are off. The fixed fields are 16 characters long for the header and argument, 5 characters long for the terminator, numbers are right justified, letters are left justified, and blanks are filled.

Example: The counter is measuring a 12.34 GHz signal. The operator enters the following messages through the controller:

```
RESOLUTION 6
OUTPUT FREQ
```

The output will be as follows (b is for blank):

| Parameter | Output |
|---|---|
| Default: | bbbbb12340000000 CR LF |
| SCIENTIFIC ON: | bbbbbbbb12.340E+9 CR LF |
| DYNAMIC ON: | 12.34E9 |
| HEADER ON: | FREQUENCY 12.34 GHz CR LF |

If the counter is searching, zero data will be output to the controller on all results once every search loop. If the counter has found a signal, a measurement result will be output only once; thus when the instrument is in HOLD, the user must trigger the counter before sending another talk address or the counter will hold indefinitely, since it has no data to output.

### SERIAL POLLING STATUS BYTE

The 625A counter maintains a one byte register that contains current information on the status of the instrument. This register, called the status byte, can be accessed through the GPIB using the serial poll command. When serial polled, the counter responds by returning a numeric value between 0 and 256. This value is the weighted sum of the status bits which are set. The status byte is structured as follows:

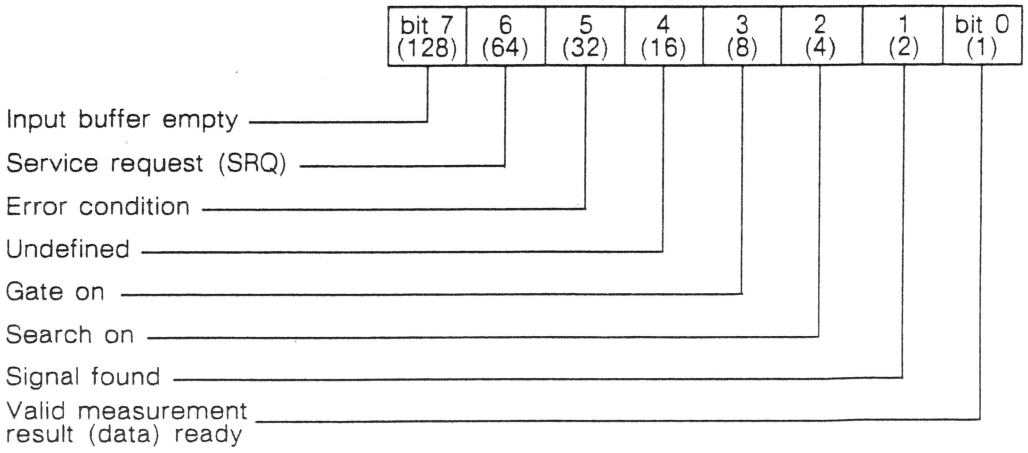



Figure 4-1. Status Byte Structure.

For example, execute the following commands using an HP Model 320.

```
10 A=SPOLL(718)
20 DISP A
30 END
```

With no signal applied to the counter, the value displayed on the HP Model 320 controller should be 132. Since the value is the weighted sum of all the bits set in the status byte, a value of 132 indicates that the GPIB input buffer is empty and the counter is in the search mode.

## SERVICE REQUEST MASKS

The counter can be instructed to send an interrupt, by setting the SRQ line on the GPIB, when any ORed combination of the bits in the status byte are set. An interrupt may also be generated when any ANDed combination of status bytes are set. These interrupts are accomplished by sending the counter service request masks.

For example, to instruct the counter to generate an SRQ whenever it has valid data available OR an error condition exists, send the following service request mask:

OUTPUT 718;"SRQMASK 33"

This tells the counter to generate an SRQ interrupt whenever bit 0 or bit 5 of the status byte are set. Since bit 0 corresponds to valid measurement result ready and bit 5 corresponds to error condition, the counter generates an SRQ whenever either an error condition exists or a valid measurement is available.

Similarly, the counter can be instructed to generate an SRQ when a signal is found AND the input buffer is empty. To accomplish this, the following service request mask can be sent:

OUTPUT 718;"ASRQMASK 130"

The counter then generates an SRQ whenever bit 1 (signal found) and bit 7 (input buffer empty) are set. The following items should be included in any program using the SRQ feature:

1. Tell the counter when to generate an SRQ. That is, tell the counter which events should generate an SRQ. This is done by using either the SRQMASK or ASRQMASK commands.

2. Tell the controller to monitor the SRQ line on the GPIB. The SRQ is a maskable interrupt and the controller needs to know if it should respond to the interrupt.

3. Tell the controller what to do when it receives an SRQ interrupt.

4. Serial poll the counter after an SRQ is generated to clear the interrupt. When the counter generates an SRQ it sets bit 6 in the status byte. Serial polling the instrument clears the SRQ bit and allows the instrument to generate a new SRQ upon the next occurrence of the conditions specified in the particular service request mask.

5. It may also be necessary to clear the SRQ register in the controller. Consult your manual on the controller for more information on clearing the SRQ register in the controller.

The following program, written on an HP 9826, demonstrates how to use the SRQ feature to obtain a valid measurement from the counter.

```
10   ASSIGN @COUNTER TO 718          ! Assigns 718 to address variable
                                     ! The number 7 is the GPIB interface
                                     ! and 18 is the counters GPIB address
20   REMOTE @COUNTER                 ! Place counter in Remote
30   OUTPUT @COUNTER;"SRQMASK 1"     ! Send SRQ mask to counter
40   ENABLE INTR 7;2                 ! Enable interrupt in controller
50   ON INTR 7 GOTO FLAG             ! Tell controller how to handle interrupt
60   WAITING:                        ! Label
70   PRINT "WAITING FOR VALID MEASUREMENT"
80   GOTO WAITING
90   FLAG: PRINT "***** SRQ RECEIVED *****"
100  ENTER @COUNTER;FREQ             ! Input Frequency from counter
110  PRINT "FREQ = ";FREQ            ! Print Frequency
120  S2 = SPOLL(@COUNTER)            ! Clear SRQ bit in counter
130  STATUS 7,4;S                    ! Clear SRQ bit in controller
```

```
140  OUTPUT @COUNTER;"SRQMASK 00"      ! Turn off SRQ mask in counter
150  OFF INTR 7                        ! Turn off interrupt in controller
160  END                               ! Program end
```

To demonstrate this program, set up counter with no signal applied and start the program. The controller should continually print out "Waiting for valid measurement." Then apply a signal. As soon as the counter finds the signal and counts it, the controller will print out the frequency of the signal.

### DEFAULT STATE (DEVICE CLEAR FEATURES)

The default state of the instrument occurs after power-up and/or hardware initialization, and after the device clear command. The customer can customize the default state of the counter through the use of Special Function 72. For more information on this feature, see page 3-18. The following table lists the factory-set default state of the counter.

| Parameter | Default State |
|---|---|
| Band | 3 |
| Center frequency | 0 |
| Clear display | Activated |
| Converter | Reset |
| Display | Enabled |
| Dynamic | Off |
| External reference | Off |
| Header | Off |
| Hold | Off |
| Internal reference | On |
| Multiply frequency | 1 |
| Offset frequency | 0 |
| Output | Frequency measurement data |
| Reset/local | Local |
| Resolution | 0 (1 Hz) |
| Sample rate | Maximum |
| Scientific | Off |
| Separate | Off |
| Special functions | Off |
| SRQmask | Off |

### GPIB ADDRESS SELECTION

This counter employs a software selectable GPIB address which is stored in nonvolatile memory. To verify the GPIB address, enter Special Function 90: the counter will display the current GPIB address. Press the CLEAR DISPLAY key to exit Special Function 90 without changing the GPIB address.

To change the GPIB address, enter Special Function 90 followed by the desired GPIB address (see table below).

PRESS: SPECIAL FUNC [9] [0] [2] [0]

Since the GPIB address is stored in nonvolatile memory, the counter will always default to the last GPIB address selected.

| ADDRESS CHARACTERS* | | ADDRESS CODES | | | | | |
|---|---|---|---|---|---|---|---|
| | | Binary | | | | | |
| Listen | Talk | 5 | 4 | 3 | 2 | 1 | Decimal** |
| SP | @ | 0 | 0 | 0 | 0 | 0 | 00 |
| ! | A | 0 | 0 | 0 | 0 | 1 | 01 |
| " | B | 0 | 0 | 0 | 1 | 0 | 02 |
| # | C | 0 | 0 | 0 | 1 | 1 | 03 |
| $ | D | 0 | 0 | 1 | 0 | 0 | 04 |
| % | E | 0 | 0 | 1 | 0 | 1 | 05 |
| & | F | 0 | 0 | 1 | 1 | 0 | 06 |
| ' | G | 0 | 0 | 1 | 1 | 1 | 07 |
| ( | H | 0 | 1 | 0 | 0 | 0 | 08 |
| ) | I | 0 | 1 | 0 | 0 | 1 | 09 |
| * | J | 0 | 1 | 0 | 1 | 0 | 10 |
| + | K | 0 | 1 | 0 | 1 | 1 | 11 |
| , | L | 0 | 1 | 1 | 0 | 0 | 12 |
| - | M | 0 | 1 | 1 | 0 | 1 | 13 |
| . | N | 0 | 1 | 1 | 1 | 0 | 14 |
| / | O | 0 | 1 | 1 | 1 | 1 | 15 |
| 0 | P | 1 | 0 | 0 | 0 | 0 | 16 |
| 1 | Q | 1 | 0 | 0 | 0 | 1 | 17 |
| 2 | R | 1 | 0 | 0 | 1 | 0 | 18 |
| 3 | S | 1 | 0 | 0 | 1 | 1 | 19 |
| 4 | T | 1 | 0 | 1 | 0 | 0 | 20 |
| 5 | U | 1 | 0 | 1 | 0 | 1 | 21 |
| 6 | V | 1 | 0 | 1 | 1 | 0 | 22 |
| 7 | W | 1 | 0 | 1 | 1 | 1 | 23 |
| 8 | X | 1 | 1 | 0 | 0 | 0 | 24 |
| 9 | Y | 1 | 1 | 0 | 0 | 1 | 25 |
| : | Z | 1 | 1 | 0 | 1 | 0 | 26 |
| ; | [ | 1 | 1 | 0 | 1 | 1 | 27 |
| < | / | 1 | 1 | 1 | 0 | 0 | 28 |
| = | ] | 1 | 1 | 1 | 0 | 1 | 29 |
| > | ^ | 1 | 1 | 1 | 1 | 0 | 30 |

* Address characters in ASCII code.

** Decimal Talk/Listen Address is provided as a cross-reference for those controllers which use decimal address.

## TALK ONLY MODES

The talk only modes enable the counter to continuously output data to other devices on the bus, such as a printer, without the need of an instrument controller. To use the counter in a talk only mode, enter the GPIB address corresponding to the desired data output format. The receiver must be configured to the listen only mode to enable data transfer across the bus.

NOTE

Address is composed of the binary value of the choices + 32.

| Scientific | Separate | Header | Dynamic | Address |
|---|---|---|---|---|
| off | off | off | off | 32 |
| off | off | off | on | 33 |
| off | off | on | off | 34 |
| off | off | on | on | 35 |
| off | on | off | off | 36 |
| off | on | off | on | 37 |
| off | on | on | off | 38 |
| off | on | on | on | 39 |
| on | off | off | off | 40 |
| on | off | off | on | 41 |
| on | off | on | off | 42 |
| on | off | on | on | 43 |
| on | on | off | off | 44 |
| on | on | off | on | 45 |
| on | on | on | off | 46 |
| on | on | on | on | 47 |

## DATA INPUT AND OUTPUT SPEED

### Input Speed

It takes a specific amount of time for the counter to process input data (due to error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus and is temporarily stored in a 256-character storage memory.

The users of the GPIB interface need to be aware of the difference between accepting data and complying with it. If the counter is asked to output a reading before it is finished processing the input data, the output will not reflect the newly entered data. To prevent this, sufficient programmed delays must be provided (see the sample program format on page 4-6). The user can also make use of the counter's status byte. Bit 7 in the status byte can be used to determine if the counter has completed the processing of the GPIB command messages. Refer to the section on the serial polling status byte.

### Output Speed

Several options have been provided in the GPIB interface for the user who wants to increase the output speed of the counter. Each of the following conditions decreases the measurement cycle time. The fastest measurement cycle time is achieved with all of the following conditions set:

HEADER OFF: Outputs the numeric results without header or terminator (default).

SCIENTIFIC OFF: Outputs fixed point results which are shorter than exponential notations (default).

DYNAMIC ON: Suppresses leading blanks. NOTE: The controller must have free field capability.

SPECIAL 61: Disables the tracking feature, thus saving the time required for YIG and VCO corrections.

SPECIAL 63: Disables sample rate control, eliminating any delay between gates. (For counter in local mode.)

SPECIAL 65: Disables the LED results display thus saving the time required for display, formatting and output.

SAMPLERATE 0: Same as SPECIAL 63 for counter in remote mode.

## READING MEASUREMENTS

To read a measurement from the counter to an instrument controller, the user must first address the counter to talk and the controller to listen. The examples below indicate how a controller may read a measurement from the counter.

- Hewlett Packard 9825A

  ```
  10 red 718,A
  20 prt A
  ```

- Hewlett Packard 9845A

  ```
  10 ENTER 718,A
  20 PRINT A
  ```

- Tektronix 4051A

  ```
  10 INPUT @ 18:A
  20 PRINT A
  ```

The EIP counter user has a choice of method for taking readings. When the command HOLD is ON, the counter takes one reading then waits for a RESET command or a device trigger GPIB command. In this condition, the counter is sent a RESET command or a device trigger and (when addressed to talk) outputs a new reading to the bus. The counter will hold that particular reading on the display until another RESET command or device trigger is received.

When the HOLD command is off, data is read out to the bus in the normal way. The display is automatically updated according to the specified sample rate, and the counter can output successive readings without requiring a RESET command or device trigger each time.

# SECTION 5
# OPERATIONAL VERIFICATION TESTS

## INTRODUCTION

This section contains information for verifying proper operation of the counter. Although these tests are not comprehensive, they do insure, to a high degree of confidence, that the instrument is operating properly. They can be useful for incoming inspection and should be performed after any servicing to insure proper operation of the counter. All tests can be performed without removing the instrument covers. A test report form is included at the end of this section that can be used to provide a test record. If the application is especially critical in nature, more extensive testing may be necessary and is covered in the performance verification test section of the service manual.

## EQUIPMENT REQUIREMENTS

Equipment required for the operational verification tests on the EIP 625A counter is listed in Table 5-1. The critical parameters are the minimum use specifications required for the performance of the procedures, and are included to assist in the selection of alternative equipment. Satisfactory performance of alternative items should be verified prior to use. All applicable equipment must bear evidence of current calibration. For many of the following tests, an EIP 578B counter is used to source lock the microwave sweeper, thus providing a stable source for testing. This combination may be replaced by a frequency synthesizer.

**Table 5-1. Equipment Requirements.**

| Description | Critical Parameters | Recommended Manufacturer | Model |
|---|---|---|---|
| Synthesized Function Generator | 10 Hz to 10 MHz | Wavetek | 23 |
| Sweep Generator | 10 MHz to 20 GHz | Wiltron | 6647B |
| Sweep Generator | 3 GHz to 18 GHz | Wiltron | 6635B |
| Source Locking Counter | 10 MHz to 20 GHz | EIP | 578B |
| Spectrum Analyzer | 3 GHz to 18 GHz | Hewlett Packard | 8566A |
| Power Meter | | Hewlett Packard | 437B |
| Power Sensor | 50 MHz to 20 GHz (-20 to +10 dBm) | Hewlett Packard | 8485B |
| Oscilloscope | DC to 100 MHz | Tektronix | 475 |
| Power Splitter | 10 MHz to 20 GHz | Hewlett Packard | 11667B |
| Directional Coupler | 950 MHz to 18 GHz | Narda | 4222-16 |
| Directional Coupler | 18 GHz to 20 GHz | Narda | 4017B-10 |
| 3 dB Attenuator | DC to 20 GHz | Weinschel | 9-3 |

## SOURCE LOCKING SETUP

In some of the following tests, the EIP 578B counter is used to source lock the sweep generator to provide a stable frequency source for testing the 625A counter.

The source locking setup, described below, is not limited to locking the Wiltron sweeper. It can be used to source lock almost any electronically tunable signal source over a frequency range of 10 MHz to 110 GHz. For more information on source locking the Wiltron 6600 series of sweep generators, request Application Bulletin 10 from our sales representative in your area or directly from EIP.

Regardless of the particular sweeper, the procedure for source locking is basically the same. A sample of the output from the sweeper is applied to the appropriate band on the EIP 578B counter. For the setup shown in Figure 5-1, a power splitter provides the sample. The COARSE TUNE OUT connector from the 578B counter is connected to the external sweep input on the sweeper. The ∅ LOCK OUT connector on the 578B counter is connected to the FM input on the sweeper. The frequency modulation on the sweeper is enabled and the sweeper is set to the external sweep mode.

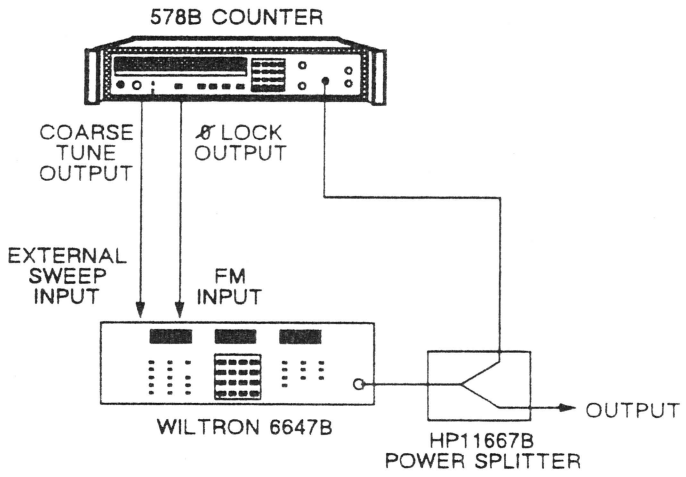



**Figure 5-1. Source Locking Setup.**

With the equipment set up as described above, source locking over the entire range of the sweeper can be achieved by entering the desired frequency.

For example, to lock the sweeper at 10 GHz:

PRESS: LOCK FREQ | 1 | 0 | GHz

At this point, the sweeper should be locked to 10 GHz, the LCK annunciator on the counter should be lit, and 10 GHz should be the displayed frequency. In the following tests, the output frequency from the sweeper is controlled directly by the EIP 578B counter, while the power is controlled at the sweeper.

# OPERATIONAL VERIFICATION TEST PROCEDURES

## BAND 1 - RANGE AND SENSITIVITY TEST

### Description

This test verifies counter operation from 10 Hz to 100 MHz at 25 mVrms (70.7 mV p-p). The oscilloscope is used to set signal levels below 10 MHz, and the power meter is used to set signal levels at 10 MHz and above. Test setup 1 tests the counter from 10 Hz to 10 MHz and test setup 2 tests the counter from 20 MHz to 100 MHz.

### Equipment

Synthesized Function Generator (Wavetek 23)
Sweep Generator (Wiltron 6647B)
Source Locking Counter (EIP 578B)
Power Meter (Hewlett Packard 437B)
Power Sensor (Hewlett Packard 8481A)
Power Splitter (Hewlett Packard 11687B)
Oscilloscope (Tektronix 475)

### Equipment Setup 1

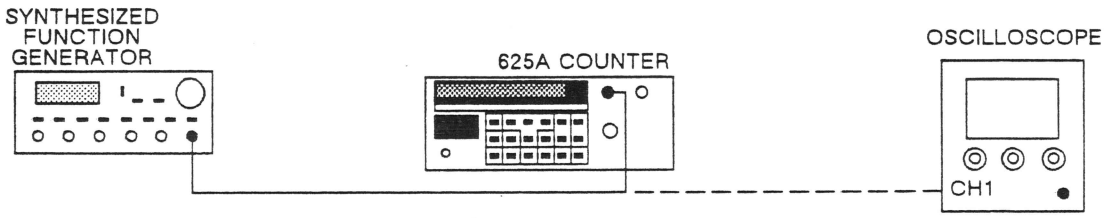



**Figure 5-2. Band 1 Range and Sensitivity Test Setup (10 Hz to 10 MHz).**

### Procedure

1. Connect equipment as shown in Figure 5-2.
2. Set the counter to Band 1 and select resolution 0 (1 Hz resolution).
3. Set the output frequency from the synthesizer to 10 Hz.
4. Using the oscilloscope, set the output signal level from the synthesizer to 70.7 mV p-p.
5. Apply the signal to the counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz.

Equipment Setup 2

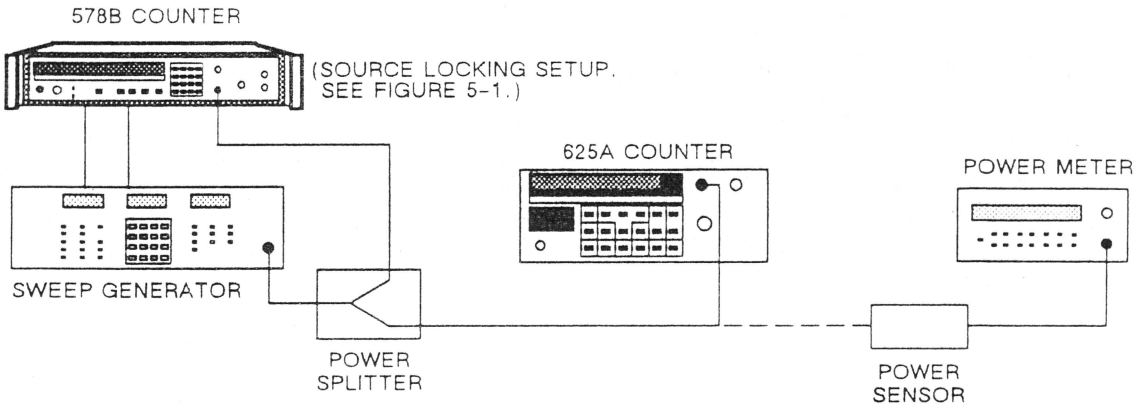



Figure 5-3. Band 1 Range and Sensitivity Test Setup (20 MHz to 100 MHz).

**Procedure**

1. Connect equipment as shown in Figure 5-3.
2. Set the 625A counter to Band 1 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 20 MHz.
4. Using the oscilloscope, set the output signal level from the sweeper to 70.7 mV p-p.
5. Apply the signal to the 625A counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 40, 80 and 100 MHz.

## BAND 2 - RANGE AND SENSITIVITY TEST

**Description**

This test verifies counter operation from 100 MHz to 1 GHz at -15 dBm. The power meter is used to set signal levels.

**Equipment**

Sweep Generator (Wiltron 6647B)
Source Locking Counter (EIP 578B)
Power Meter (Hewlett Packard 437B)
Power Sensor (Hewlett Packard 8481A)
Power Splitter (Hewlett Packard 11667B)

**Procedure**

1. Connect equipment as shown in Figure 5-4.
2. Set the 625A counter to Band 2 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 100 MHz.
4. Using the power meter, set the output signal level from the sweeper to -15 dBm.
5. Apply the signal to the counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 300, 500, 700, and 900 MHz and 1 GHz.

### Equipment Setup

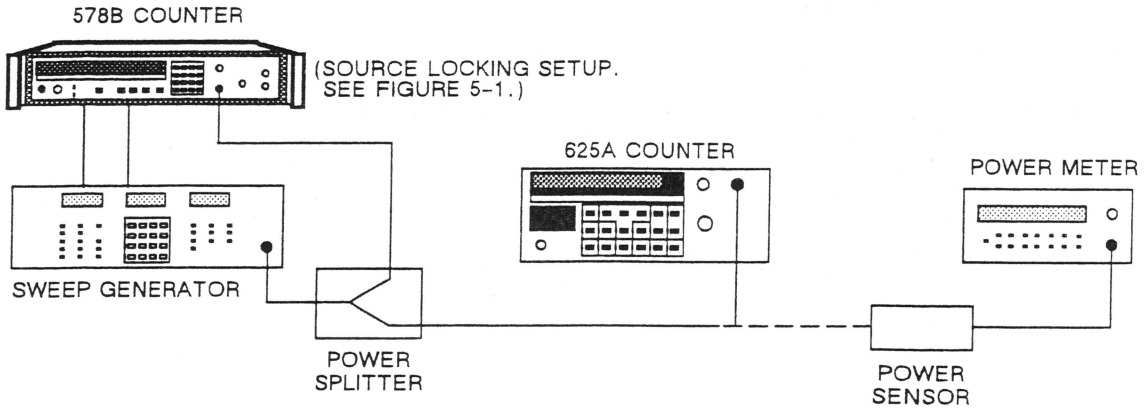



**Figure 5-4. Band 2 Range and Sensitivity Test Setup.**

## BAND 3 - RANGE AND SENSITIVITY TEST

### Description

This test verifies counter operation from 950 MHz to 20 GHz.

### Equipment

Sweep Generator (Wiltron 6647B)
Source Locking Counter (EIP 578B)
Power Meter (Hewlett Packard 437B)
Power Sensor (Hewlett Packard 8485B)
Power Splitter (Hewlett Packard 11667B)
Directional Coupler (Narda 4222-16)
Directional Coupler (Narda 4017B-10)
3 dB Attenuator (2) (Weinschel 9-3)

### Equipment Setup

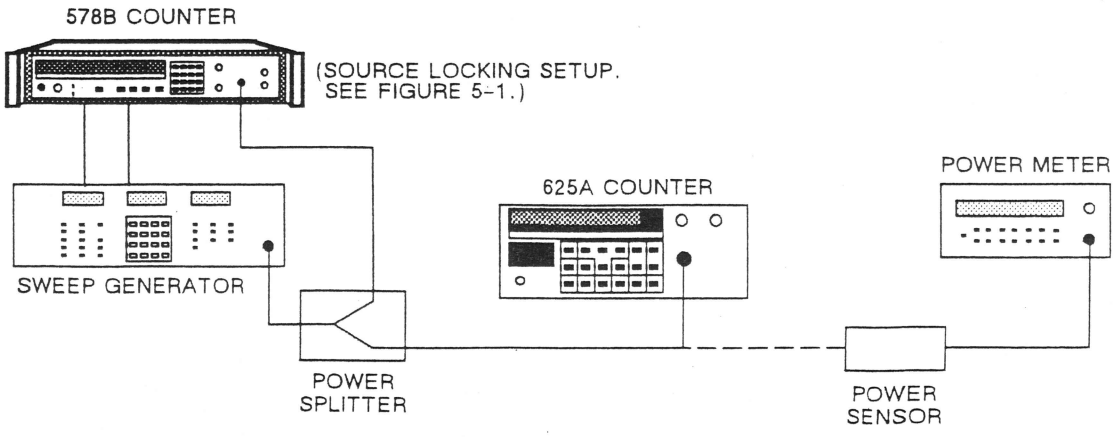



**Figure 5-5. Band 3 CW Signal Range and Sensitivity Test Setup.**

### Procedure

1. Connect equipment as shown in Figure 5-5.
2. Set the counter to Band 3 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 950 MHz.
4. Using the power meter, set the output signal level from the sweeper to -25 dBm.
5. Apply the signal to the 625A counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 1, 3, 6, 10, and 12.4 GHz.
7. Using the EIP 578B counter, source lock the sweeper at 13 GHz.
8. Using the power meter, set the output signal level from the sweeper to -20 dBm.
9. Apply the signal to the 625A counter, verify proper reading, and record the results.
10. Repeat steps 7, 8, and 9 at 15, 18, and 20 GHz.

## BAND 3 - AMPLITUDE DISCRIMINATION TEST

### Description

This test verifies that the counter will measure accurately the larger of two signals differing in frequency by ≥100 MHz and differing in amplitude by ≥10 dB.

### Equipment

Sweep Generator (Wiltron 6647B)
Sweep Generator (Wiltron 6635B)
Spectrum Analyzer (Hewlett Packard 8566A)
Power Splitter (Hewlett Packard 11667B)

### Equipment Setup

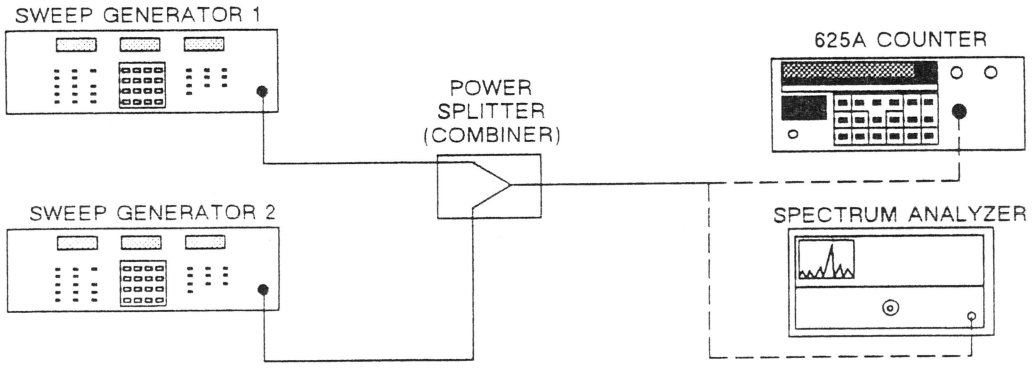



Figure 5-6. Band 3 Amplitude Discrimination Test Setup.

### Procedure

1. Connect equipment as shown in Figure 5-6.
2. Set signal generator 1 to 3.0 GHz at 0 dBm and set signal generator 2 to 3.1 GHz at +6 dBm.
3. Using the spectrum analyzer, adjust the generator power levels so that the signal amplitude difference is 10 dB.
4. Verify that the counter correctly measures the frequency of the higher power signal source.
5. Repeat steps 2, 3, and 4 at 6 and 6.1 GHz, at 12 and 12.1 GHz, and at 17.9 and 18 GHz.

## OPERATIONAL TEST RECORD

DATE: _____

MODEL: 625A SERIAL NO.: _____ CCN: _____

| TEST | | ACTUAL | SPECIFICATIONS |
|---|---|---|---|
| BAND 1 RANGE AND SENSITIVITY TEST | | | 10 Hz TO 100 MHz |
| INPUT SENSITIVITY | 10 Hz | _____ | 25 mVrms |
| | 100 Hz | _____ | |
| | 1 kHz | _____ | |
| | 10 kHz | _____ | |
| | 100 kHz | _____ | |
| | 1 MHz | _____ | |
| | 10 MHz | _____ | |
| | 20 MHz | _____ | |
| | 40 MHz | _____ | |
| | 80 MHz | _____ | |
| | 100 MHz | _____ | |
| BAND 2 RANGE AND SENSITIVITY TEST | | | 100 MHz TO 1 GHz |
| INPUT SENSITIVITY | 100 MHz | _____ | -15 dBm |
| | 300 MHz | _____ | |
| | 500 MHz | _____ | |
| | 700 MHz | _____ | |
| | 900 MHz | _____ | |
| | 1 GHz | _____ | |
| BAND 3 RANGE AND SENSITIVITY TEST | | | 950 MHz TO 20 GHz |
| INPUT SENSITIVITY | 950 MHz | _____ | -25 dBm |
| | 1 GHz | _____ | |
| | 3 GHz | _____ | |
| | 6 GHz | _____ | |
| | 10 GHz | _____ | |
| | 12.4 GHz | _____ | |
| INPUT SENSITIVITY | 13 GHz | _____ | -20 dBm |
| | 15 GHz | _____ | |
| | 18 GHz | _____ | |
| | 20 GHz | _____ | |

BAND 3 AMPLITUDE DISCRIMINATION TEST CONDITIONS: F1 > F2 BY 10 dB OR MORE.

| F1 | F2 | PASS | FAIL | |
|---|---|---|---|---|
| 3 GHz | 3.1 GHz | _____ | _____ | 10 dB |
| 6 GHz | 6.1 GHz | _____ | _____ | |
| 12 GHz | 12.1 GHz | _____ | _____ | |
| 17.9 GHz | 18 GHz | _____ | _____ | |

# SECTION 6
# THEORY OF OPERATION

## INTRODUCTION

The 625A microwave counter is a microprocessor-based multifunction instrument that automatically measures CW signals in the frequency range of 10 Hz to 20 GHz.

All major functions are controlled through the 18-key, functionally-grouped keyboard. Information is output via a 12-digit, sectionalized LED frequency display and a 13-message LED annunciator bank.

Microprocessor control and the unique architecture permit not only the major counter functions such as frequency offsets and frequency multiplier capabilities, but also a variety of special functions such as internal diagnostics, calibration and test aids, and sophisticated operational enhancements.

All front panel controls, except the POWER switch, and all background functions are externally programmable via the IEEE 488 - 1978 standard GPIB (General Purpose Interface Bus). Additionally, all displayed information, as well as counter setup status, is accessible via the GPIB.

The counter can best be understood by dividing it up into the following major sections: the basic counter, the RF converters for Bands 1 and 2, and the Band 3 Microwave Converter.

## BASIC COUNTER

The basic counter, shown in Figure 6-1, receives input signals from all three bands and performs frequency measurements. The basic counter can directly measure the frequency of signals from 10 Hz to 250 MHz.

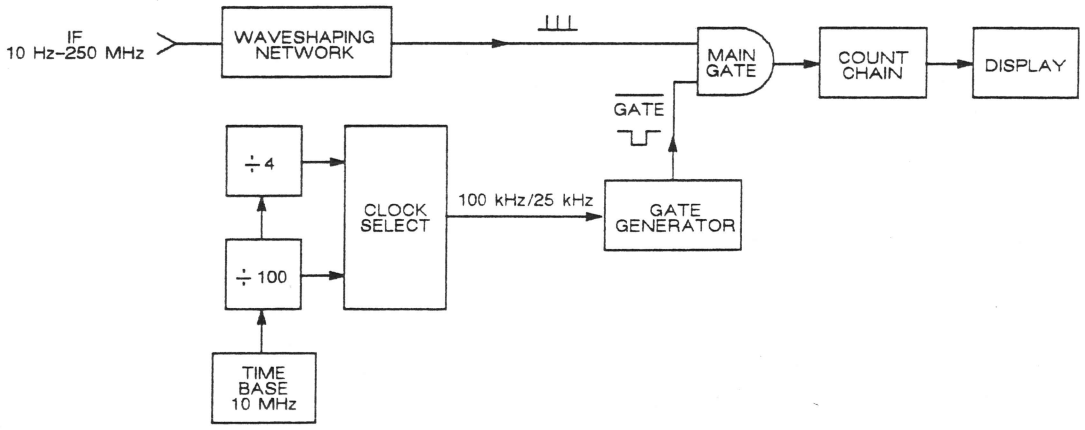



**Figure 6-1. Functional Block Diagram of Basic Counter.**

Overall operation of the counter is controlled by Processor/GPIB assembly, A5. This assembly contains a Motorola 68B09 microprocessor, its control logic, the system memory, and the circuitry for the GPIB interface. It communicates with all other assemblies in the counter via a triple bus system: the data bus, address bus, and control bus. Each assembly (except for the Signal Conditioner) contains a peripheral interface adapter (PIA) that provides the interface between the bus system and the counter hardware.

Frequency measurements are performed by comparing the unknown signal to a reference frequency output by the time base. The standard time base is a 10 MHz temperature-compensated crystal oscillator (TCXO). An optional high-stability oven oscillator is also available for improved frequency accuracy. For coherence with system clocks, the 625A has the capability of accepting an external 10 MHz reference.

A frequency measurement is made by generating a gate time consisting of a number of cycles of the reference. This gate time is used as a time interval during which the input signal is counted.

## RF CONVERTERS

### BAND 1 CONVERTER

Signals between 10 Hz and 100 MHz require no prescaling and are directly counted. The Band 1 signal is first processed by the signal conditioner assembly (A9). The output is then sent to the basic counter, the measurements performed, and the measurement results displayed. Figure 6-2 is a functional block diagram of the Band 1 circuitry.

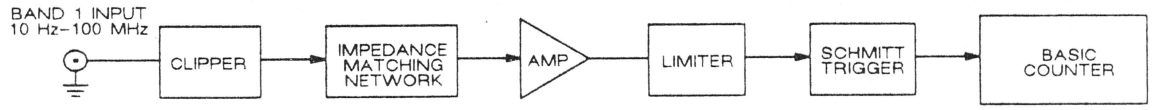



**Figure 6-2. Band 1 Converter Functional Block Diagram.**

### BAND 2 CONVERTER

Signals between 250 MHz and 1 GHz are prescaled by four before reaching the basic counter. In this mode, the gate is made four times longer to compensate for the prescaled signal. While Band 2 is selected, the counter continuously monitors the input for a signal. When a signal is detected, the threshold detector causes the counter to generate a gate signal and the frequency of the signal is measured. To provide the wide dynamic range without distortion, an AGC (automatic gain control) circuit is used. This circuit adjusts the attenuation of the input attenuator to maintain an optimum signal level. Figure 6-3 is a functional block diagram of the Band 2 converter, and Figure 6-4 is a flow diagram of the Band 2 measurement routine.

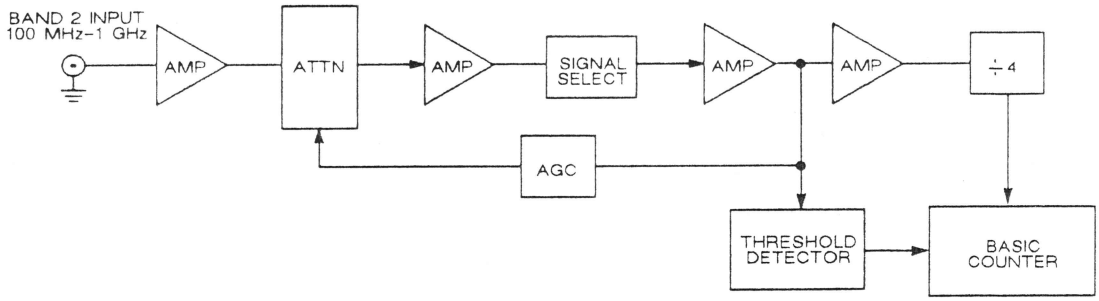



Figure 6-3. Band 2 Converter Functional Block Diagram.

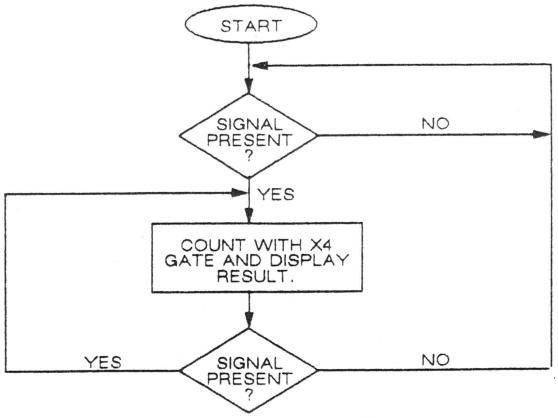



**Figure 6-4. Band 2 Converter Lock Process Flow Diagram.**

## BAND 3 MICROWAVE CONVERTER

Frequency measurement in the microwave band is accomplished by down converting the microwave signal to an IF signal of approximately 120 MHz. A narrow bandpass microwave filter (YIG filter) is used on this band to eliminate all but the desired microwave signal prior to down conversion. Figure 6-5 is a functional block diagram of the Band 3 converter, and Figure 6-6 is a flow diagram showing converter operation.

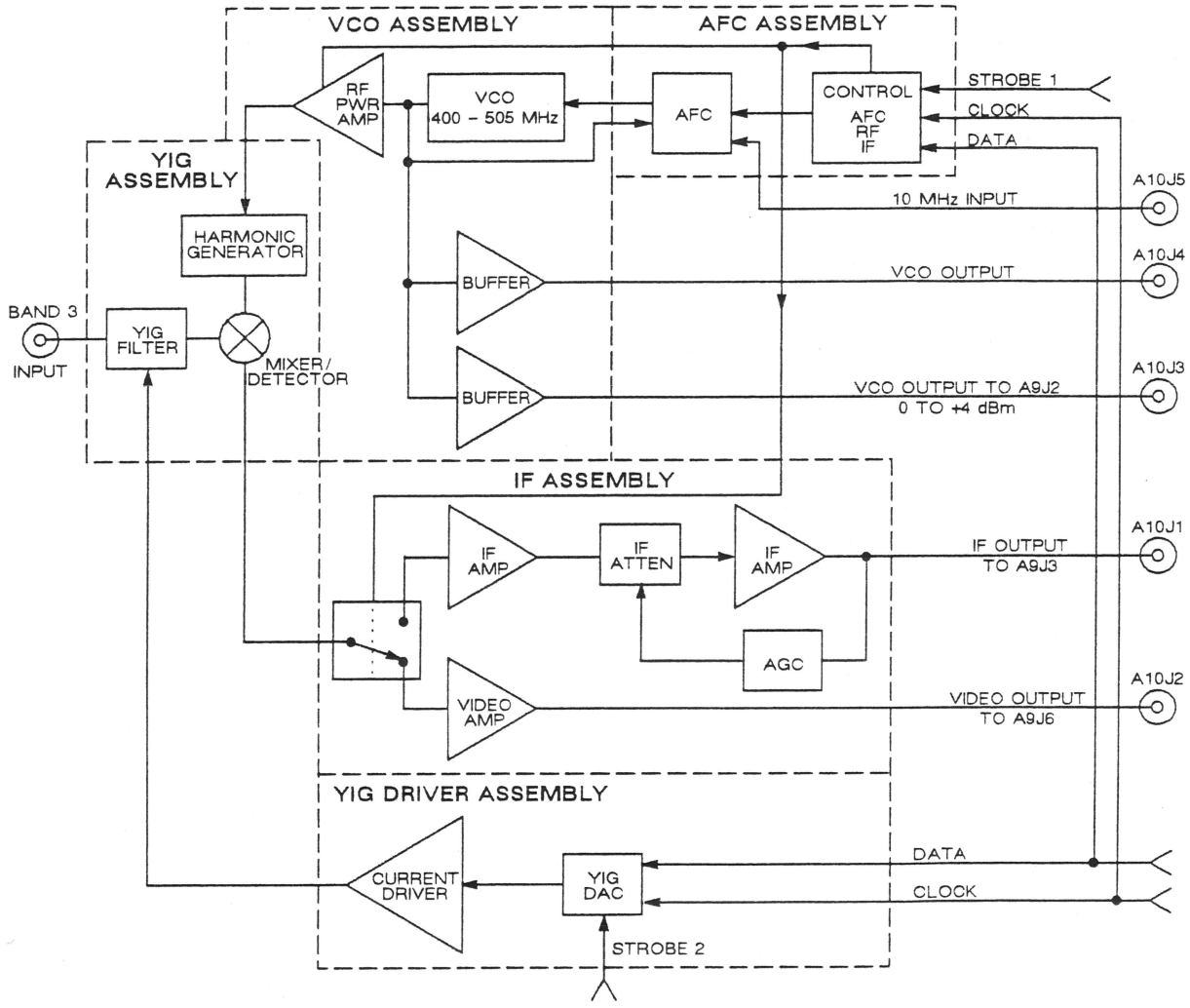



**Figure 6-5. Band 3 Microwave Converter Functional Block Diagram.**

The actual process of signal measurement in the microwave band is accomplished using a series of steps:

1. Search for the largest signal.
2. Center the YIG on the largest signal.
3. Calculate the harmonic number and required VCO frequency.
4. Measure the IF.
5. Perform calculations.
6. Display measurement.

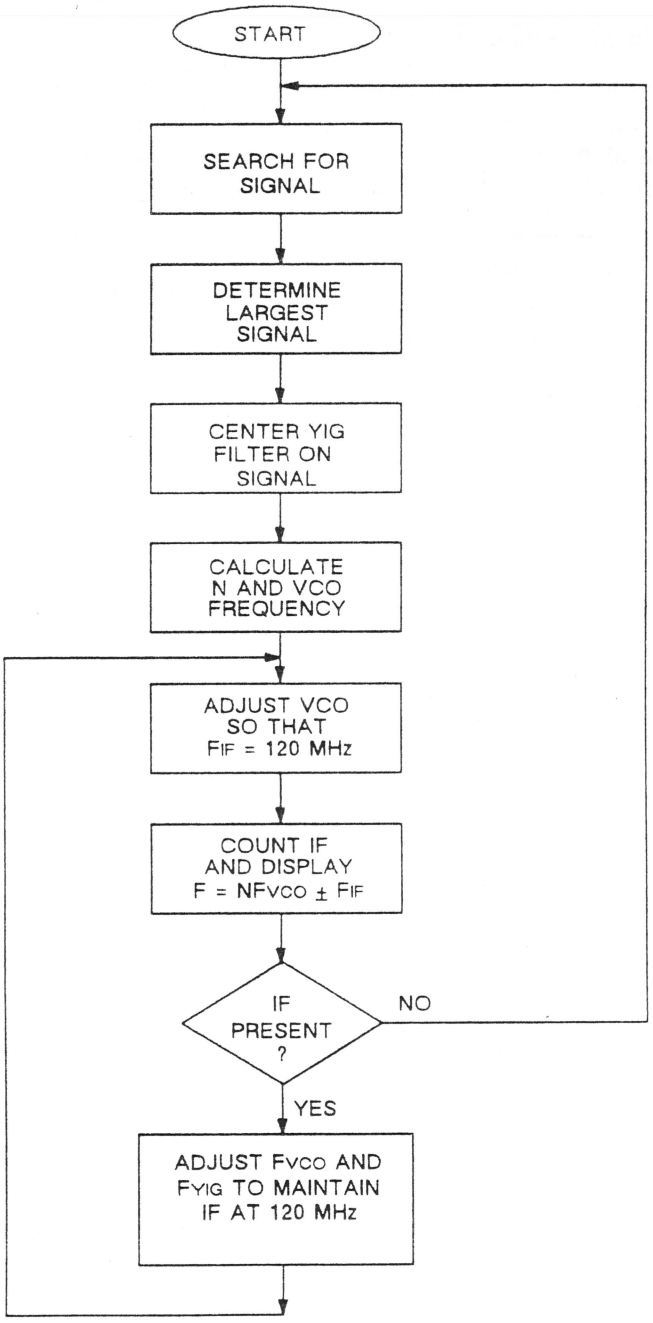



Figure 6-6. Microwave Converter Operation Flow Diagram.

During the search routine, the counter selects the largest signal present within the selected, or default range of the Band 3 input. During this routine, the YIG filter, a narrow bandpass electronically tunable microwave filter at the input to Band 3, is continuously swept from the low limit to the high limit. During this time, the Band 3 local oscillator is turned off and the microwave mixer at the output of the YIG filter is used as a microwave detector. The output from the mixer is applied to the video amplifier which feeds a 16 bit flash A/D converter, with a resolution of approximately 6 dB. The A/D converter continuously converts the detected signal into a 16 bit digital word. The least significant bit on the A/D is tied to an interrupt line so, if a signal is found while the YIG filter is sweeping across the band, an interrupt will be generated. The microprocessor responds to the interrupt by stopping the YIG filter at that point in the sweep. The microprocessor then reads the YIG DAC setting and relative amplitude from the flash A/D and stores it in memory. The counter than continues the sweep. If other signals are detected, their relative amplitudes are compared with the stored information. If the new signal is higher in amplitude, the memory is updated with information on the new signal. After searching the entire band, the YIG DAC setting and relative amplitude of the highest signal present are stored in memory.

The next step is to precisely center the YIG on the selected signal. This process begins by moving the YIG to the signal selected during the search routine. The YIG is then stepped in 2 MHz steps around the signal until two points are found: the points on either side of the peak 3 dB down from the peak. From these points the approximate "center of mass frequency" of the signal is found, and the YIG filter is set to that frequency.

After the YIG is centered on the signal, the harmonic number N is calculated based on the setting of the YIG filter using the following formula:

$$N = \frac{F_{YIG} - 120\ MHz}{500\ MHz}$$

The resulting N is rounded up to the next higher integer. At this point low side mixing is assumed, and the proper VCO frequency is calculated using the formula:

$$F_{VCO} = \frac{F_{YIG} - 120\ MHz}{N}$$

If the results yield a VCO frequency which is less than 400 MHz (the minimum VCO frequency), high side mixing is assumed, and $F_{VCO}$ is recalculated using the formula:

$$F_{VCO} = \frac{F_{YIG} + 120\ MHz}{N}$$

Since $F_{YIG}$ is only approximately equal to $F_{IN}$, the frequency will not be exactly 120 MHz. Therefore, the next step is to adjust the VCO to shift $F_{IN}$ into the middle of the IF passband by counting $F_{IF}$ and adjusting $F_{VCO}$ as follows:

$$\Delta F_{VCO} = \frac{\pm F_{IF} - 120\ MHz}{N}$$

Where: $+F_{IF}$ is used if low side mixing and
$-F_{IF}$ is used if high side mixing.

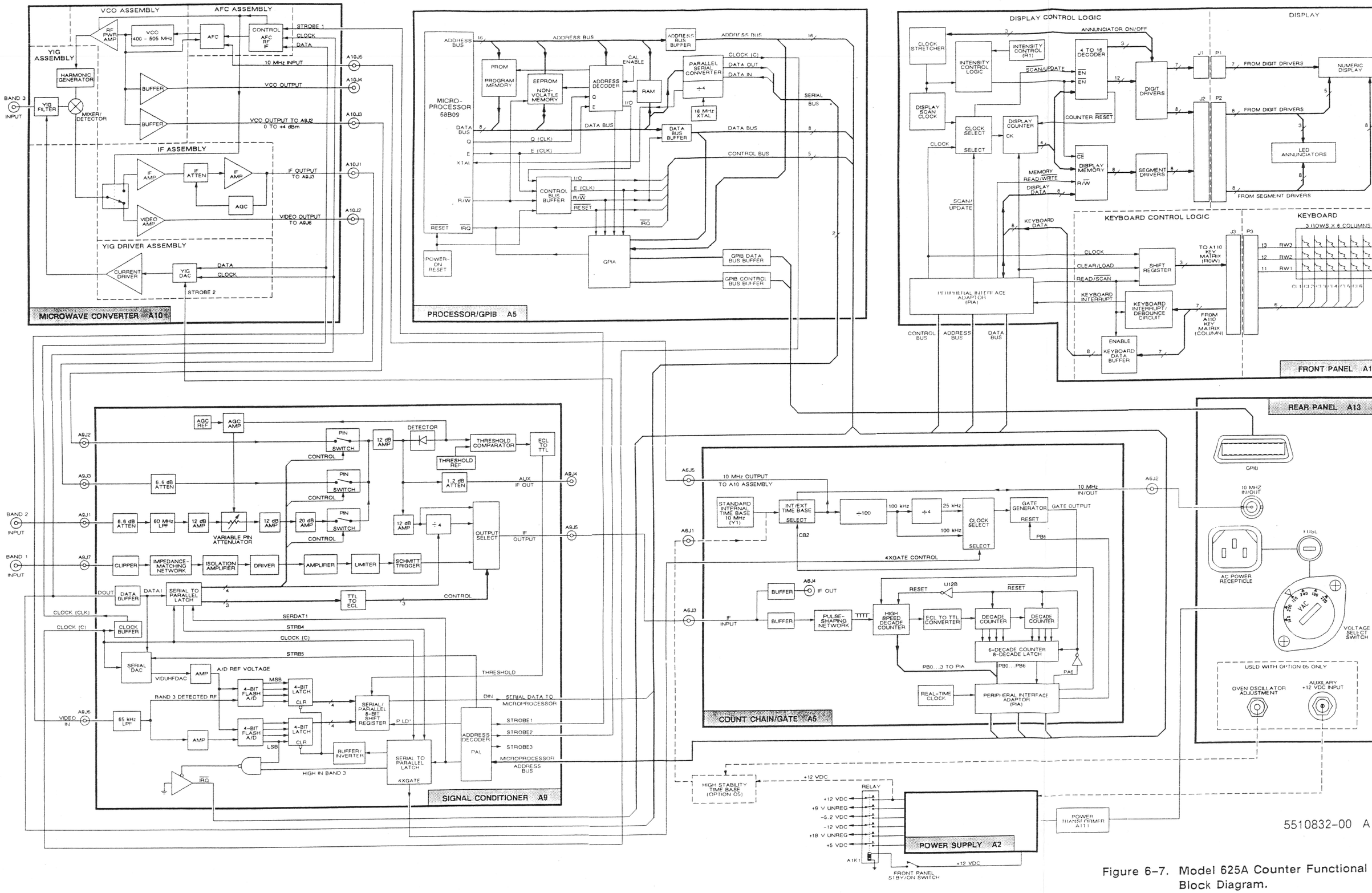
Once the VCO corrections have been made, the counter counts the IF and calculates the input frequency using the following formula:

$$F_{IN} = N \times F_{VCO} \pm F_{IF}$$

Where: N = Harmonic number
FVCO = VCO frequency
± = + for low side mixing
– for high side mixing

and the results are displayed.

After each measurement, new frequencies for the YIG and VCO are calculated to maintain the IF at 120 MHz. This method provides rapid tracking of a signal being tuned.




5510832-00 A

Figure 6-7. Model 625A Counter Functional Block Diagram.

# SECTION 7
# ADJUSTMENT AND CALIBRATION

## INTRODUCTION

The following procedures are used to adjust and calibrate the EIP 625A counter. The recommended calibration interval is six months. Adjustments within this time interval should be made if the counter does not operate as specified, or if it has been repaired. If the adjustments do not result in the specified performance, refer to the troubleshooting section of this manual.

The following is a list of the adjustment and calibration procedures described in this section:

- Power supply adjustment
- Display intensity adjustment
- Time base calibration
- Band 3 YIG DAC calibration

Table 7-1 lists the functions, specifications, and methods used when performing the adjustment and calibration routines. Figure 7-1 shows the locations of the adjustment controls. (Note: for additional information on PCB assembly component or test point (TP) locations, refer to Section 10 of this manual.)

**Table 7-1. Adjustment and Calibration Procedures.**

| Function | Performance Specification | Method |
|---|---|---|
| Power Supply | Voltage between A2TP1 (+12 V) and ground is +12 ±0.05 V | Adjust A2R3; verify with DVM. |
| | Voltage between A2TP2 (-12 V) and ground is -12 ±0.05 V | Adjust A2R6; verify with DVM. |
| | Voltage between A2TP3 (-5.2 V) and ground is -5.2 ±0.25 V | Verify with DVM. |
| | Voltage between A2TP4 (+5 V) and ground is +5 ±0.25 V | Verify with DVM. |
| Time Base Adjustment | Adjust the output frequency of the TCXO to 10 MHz ±1 Hz | On A6, turn the TCXO adjustment screw to set frequency using frequency standard as a reference. |
| YIG DAC Calibration | Automatic calibration of DAC to YIG filter | Use Special Function 91. |
| Display Intensity | LED brightness level is adjusted to suit operator's comfort | Adjust A12A2R1 on Front Panel Display/ Logic board. |

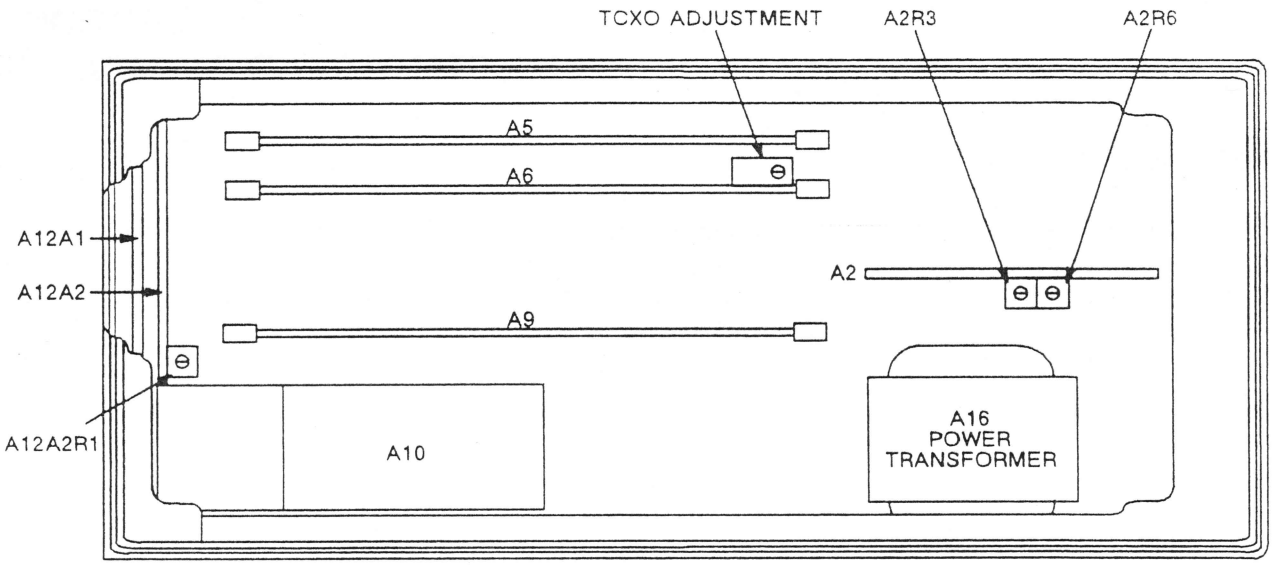



**Figure 7-1. Adjustment Control Locations.**

## EQUIPMENT REQUIRED

Table 7-2 provides a list of equipment for use in performing the adjustment and calibration procedures detailed in this section. The critical parameters listed are minimum use specifications required for calibration, and are included to assist in selecting alternative equipment. Satisfactory performance of alternative equipment should be verified prior to use, and all applicable equipment must bear evidence of current calibration.

**Table 7-2. Equipment Required.**

| Description | Critical Parameters | Recommended Manufacturer | Model |
|---|---|---|---|
| Microwave Counter | 0.1 Hz resolution | EIP | 545B |
| Digital Voltmeter | 4 1/2 digit resolution | Fluke | 8050A |
| 50 ohm Feedthrough Termination | 50 ohms resistance | Pamona | 4119-50 |
| Oscilloscope | 100 MHz bandwidth | Tektronix | 475 |
| Microwave Synthesizer | 2 GHz to 18 GHz | HP | 8340A |
| Power Meter | 2 GHz to 18 GHz | HP | 436A |
| Power Sensor | 2 GHz to 18 GHz | HP | 8485A |
| Frequency Standard | Short term stability $\geq 1 \times 10^{-11}$ | Stanford Research | FS700 with Option 01 |

## PRELIMINARY OPERATIONS

### WARNING

**All adjustments and calibrations described in this section must be performed with power applied to the counter and the top cover removed. Some of the instrument components carry high voltages that can, if contacted, result in personal injury. Extreme caution must therefore be exercised whenever the covers are removed. Only a qualified technician who is aware of the hazards involved should perform the following operations.**

Before any adjustments or calibrations can be performed, the top and bottom covers on the 625A counter must be removed. To remove the covers, perform the following:

Remove the 12 screws from each cover of the 625A. From the rear of the counter, insert a small screwdriver (or similar tool) into one of the 5/16 in. holes located near the corner of the rear frame assembly and gently push to dislodge the cover.

Before starting calibration, set all counter controls to their default values by performing the following:

1. Press the SPEC FUNC key on the front panel keyboard.
2. Press the "7" key followed by the "2" key to call Special Function 72.
3. Press the CLEAR DATA key on the front panel. This sets all counter parameters to their default values.

Review each procedure carefully before proceeding with adjustments or calibrations.

## ADJUSTMENTS

### POWER SUPPLY ADJUSTMENT

#### Description

This procedure describes the steps required to adjust the +12 V and the -12 V supplies, and how to check the +5 V and -5.2 V supplies located on Power Supply assembly A2. The test points listed are accessible from the bottom of the counter.

#### Equipment

Digital voltmeter (Fluke 8050A)

#### Equipment Setup

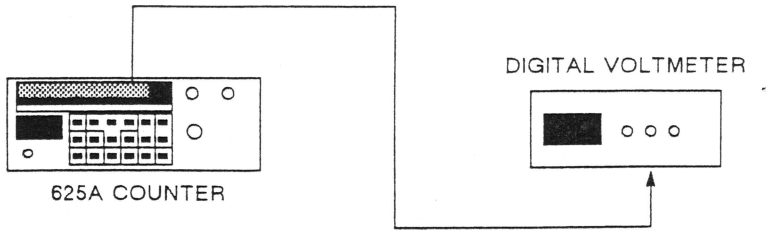



**Figure 7-2. Power Supply Adjustment Setup.**

### Procedure

1. Set up equipment as shown in Figure 7-2 and as described below.
2. Turn the counter on and allow it to warm up for 30 minutes.
3. On PCB assembly A2, connect the digital voltmeter between TP1 (+12 V) and ground.
4. Using the voltmeter, verify that the voltage is +12 V ±0.05 V. If not, adjust R3.
5. On PCB assembly A2, connect the digital voltmeter between TP2 (-12 V) and ground.
6. Using the voltmeter, verify that the voltage is -12 V ±0.05 V. If not, adjust R6.
7. On PCB assembly A2, connect the voltmeter between TP3 (-5.2 V) and ground.
8. Using the voltmeter, verify that the voltage is -5.2 V ±.25 V.
9. On PCB assembly A2, connect the voltmeter between TP4 (+5 V) and ground.
10. Using the voltmeter, verify that the voltage is +5 V ±.25 V.

## DISPLAY INTENSITY ADJUSTMENT

### Description

This procedure describes the method used to adjust the front panel display intensity. The adjustment is optional and is for viewer comfort only; it does not affect counter performance.

### Procedure

1. Turn the counter on.
2. On PCB assembly A12A2, use a screwdriver (or similar tool) to adjust potentiometer R1 to set the front panel display intensity level for the most comfortable viewing.

# CALIBRATION

## TIME BASE CALIBRATION

NOTE

The following calibration procedure applies only to 625A counters equipped with the standard TCXO time base. For instruments equipped with the high stability oven oscillator (Option 05), refer to the Options section of this manual.

### Description

The accuracy of the TCXO time base directly affects the measurement accuracy of the 625A counter. From the time an oscillator is set to its specified frequency, it will begin drifting. The magnitude of the frequency drift is specified as the aging rate of the oscillator. Time base calibration removes the frequency error due to the oscillator aging rate. Calibration of the time base is recommended once every six months. When measuring a 20 GHz signal at the end of the six-month calibration interval, measurement error due to aging rate may be as much as ±12 kHz.

**NOTE**

Two procedures are given for calibration of the TCXO time base. The first method will provide more accurate measurements when the counter is operated at 25° C only. The second method is used when the counter is to be operated over the temperature range of 0° to 50° C.

**Method 1**

In the following procedure, the time base is calibrated against a frequency standard, using an oscilloscope. The 10 MHz frequency standard is used to trigger the oscilloscope while the 10 MHz signal from the counter is applied to channel 1 of the oscilloscope. Since the oscilloscope is triggered by the frequency standard, any difference in frequency between the 10 MHz frequency standard and the 10 MHz from the counter causes the displayed signal trace to move to the left or to the right. The rate of the signal trace movement is directly proportional to the frequency difference between the frequency standard and the time base in the counter. The fractional time base error can be calculated using the following formula:

Fractional Time Base Error = (movement in cm per second) x (time per division)

For example, if the sweep speed of the oscilloscope is set to 1 μs per division, and the signal is drifting at a rate of 2 cm per second, then the fractional time base error is calculated as follows:

$$\text{Fractional Time Base Error} = \frac{2\ \text{cm}}{\text{s}} \times \frac{1 \times 10^{-6}\ \text{s}}{\text{cm}} = 2 \times 10^{-6}$$

The actual time base error in Hz is calculated by multiplying the fractional time base error by the frequency of the frequency standard, as follows:

$$\text{Time Base Error (Hz)} = \pm[(2 \times 10^{-6}) \times (10 \times 10^{6})] = \pm 20\ \text{Hz}$$

The counter measurement error is calculated by multiplying the fractional time base error by the frequency of the signal being measured. For example, if the fractional time base error is $2 \times 10^{-6}$, then the measurement error on a 20 GHz signal is calculated as follows:

$$\text{Measurement Error (Hz)} = \pm[(2 \times 10^{-6}) \times (20 \times 10^{9})] = \pm 40\ \text{kHz}$$

Equipment

Frequency standard (Stanford Research Systems FS700)
Oscilloscope (Tektronix 475)
50 ohm termination (Pamona 4119-50)

Equipment Setup

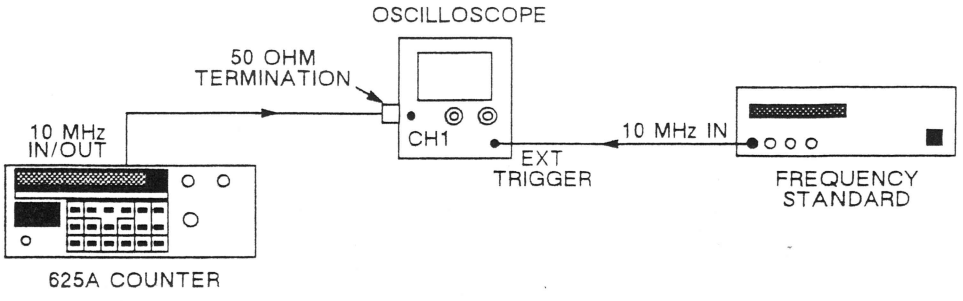



**Figure 7-3. Time Base Calibration Setup for Operation at 25° C.**

Procedure

1. Turn on the EIP 625A counter and allow a warm up period of at least 30 minutes prior to calibrating the time base.

2. Set up the equipment as shown in Figure 7-3 and as described below.

3. Connect the frequency standard output to the external trigger input on the oscilloscope. Connect the 10 MHz IN/OUT connector from the rear panel of the 625A through a 50 ohm feedthrough to the channel 1 input of the oscilloscope.

4. Set the oscilloscope to external trigger.

5. Set the oscilloscope sweep speed to 1 μs per cm.

6. While monitoring the 10 MHz time base signal from the 625A on the oscilloscope, adjust the time base (by turning the TCXO adjustment shown in Figure 7-1) until the horizontal movement rate is ≤1 centimeter in 10 seconds. This sets the time base to an accuracy of $1 \times 10^{-7}$ (10 MHz ±1 Hz).

**Method 2**

The following calibration procedure is used when the counter is to be operated over the temperature range of 0° to 50° C and should be performed at 25° C.

Equipment

Microwave counter (EIP 545B)
50 ohm termination (Pamona 4119-50)
Frequency standard (Stanford Research Systems FS700)

Equipment Setup

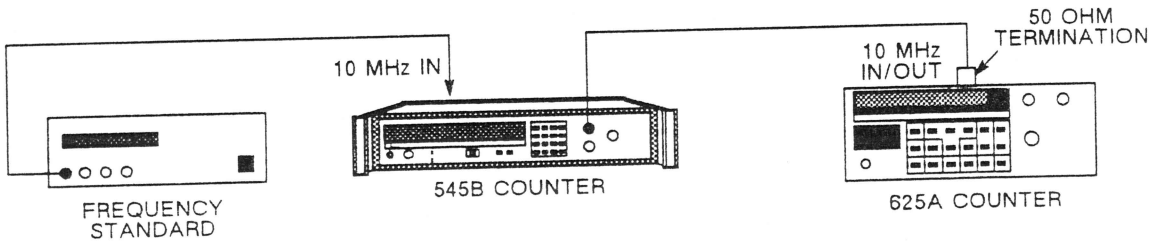



**Figure 7-4. Time Base Calibration Setup for Operation from 0° to 50° C.**

Procedure

1. Turn the 625A counter on and allow it to warm up for 30 minutes.

2. Connect the 10 MHz IN/OUT connector on the rear panel of the 625A through a 50 ohm feedthrough termination to the BAND 1 input of an EIP 545B counter.

3. Connect a 10 MHz standard to the 10 MHz IN/OUT (external reference) connector on the rear panel of the 545B counter. On the 545B counter, set the rear panel 10 MHz INT/EXT switch to EXT.

4. On the 545B, use 1 Hz resolution (1 second gate time) for coarse adjustment and 0.1 Hz resolution (10 second gate time) for fine adjustment of the TCXO frequency.

5. While monitoring the TCXO signal frequency from the 625A, displayed on the front panel of the 545B, turn the TCXO adjustment to set the TCXO frequency to 10 MHz plus the frequency offset labeled on the TCXO cover. For example, if the frequency offset on the TCXO cover is -3.5 Hz, then the TCXO frequency is adjusted to 10 MHz + (-3.5) Hz which equals 9.9999965 MHz. Likewise, if the TCXO frequency offset is +2.0 Hz, then the TCXO frequency is adjusted to 10 MHz + (2.0) Hz which equals 10.000002 MHz.

## BAND 3 YIG DAC CALIBRATION - SPECIAL FUNCTION 91

### Description

The counter uses an electronically-tuned bandpass YIG filter on the BAND 3 microwave input. The frequency to which the filter is tuned is controlled by a digital-to-analog converter (DAC). The following YIG DAC calibration procedure develops a table of correction factors that correlates the digital information sent to the DAC with the frequency to which the YIG filter is tuned.

When Special Function 91 is activated, the counter displays "F1" and measures a user-supplied 2 GHz input. The counter then displays "F2" until the "." (trigger) key is pressed, indicating that the frequency has been changed to 18 GHz. After measuring the 18 GHz input, the counter then calculates and stores (in nonvolatile memory) the correction factors for the YIG DAC.

### CAUTION

**In order to operate Special Function 91 and calibrate the YIG DAC, the RAM memory protect feature on processor assembly A5 must first be disabled. Although the counter cannot be damaged by using Special Function 91, improper use of this function may result in loss of calibration and configuration data, rendering the counter unusable until it can be recalibrated. To insure the proper use of Special Function 91, the following procedure must be strictly followed.**

### Equipment

Microwave synthesizer (Hewlett Packard 8340A)
Power meter (Hewlett Packard 436A)
Power sensor (Hewlett Packard 8485A)

### Equipment setup

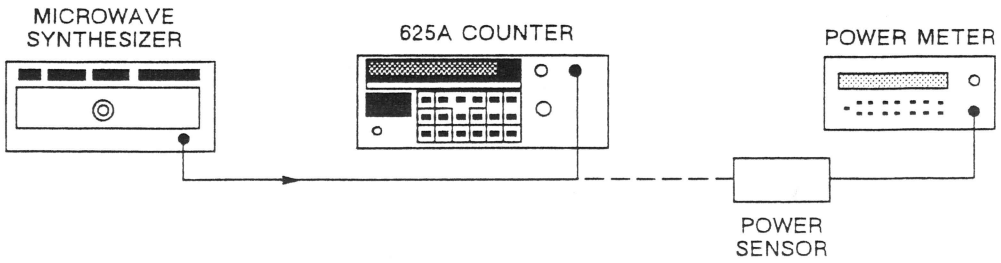



Figure 7-5. Band 3 YIG DAC Calibration Setup.

### Procedure

1. Set the POWER switch of the 625A to STBY.

2. On PCB assembly A5, attach a jumper lead between TP6 and TP7 to allow calibration data to be written to the nonvolatile memory.

3. Set the POWER switch of the 625A to ON.
4. Set up the equipment as shown in Figure 7-5 and as described below.
5. Apply a 2 GHz CW signal at 0 dBm to the BAND 3 input of the 625A.
6. Call Special Function 91 by first pressing the SPEC FUNC key, followed by the 9 key and then the 1 key.
7. When the counter displays "F1," press the "." (trigger) key.
8. When the counter display changes to "F2," apply an 18 GHz CW signal at 0 dBm to the BAND 3 input of the 625A counter.
9. Press the "." (trigger) key.
10. When the display returns to normal, the YIG DAC calibration is complete. Normal counter operation automatically resumes.
11. Set the POWER switch of the 625A to STBY.
12. On assembly A5, remove the jumper lead from TP6 to TP7. This enables the memory-protect feature on the processor assembly.
13. Replace the top cover and screws.
14. Set the POWER switch on the 625A to ON.

# SECTION 8
# PERFORMANCE VERIFICATION TESTS

## INTRODUCTION

This section describes the performance verification test procedures for the EIP Model 625A CW Microwave Counter. Test methods are summarized in Table 8-1.

**Table 8-1. Performance Verification Test Methods.**

| Counter Characteristic | Performance Specifications | Test Method |
|---|---|---|
| **Frequency Range** | | |
| Band 1 | | |
| 10 Hz to 100 MHz | Counter accurately measures over entire range. | Checked by verifying that counter displays accurate reading of frequency input from synthesized signal generator. |
| Band 2 | | |
| 100 MHz to 1 GHz | Counter accurately measures over entire range. | Checked by verifying that counter displays accurate reading of frequency input from synthesized signal generator. |
| Band 3 | | |
| 950 MHz to 20 GHz | Counter accurately measures over entire range. | Checked by verifying that counter displays accurate reading of frequency input from synthesized signal generator. |
| **Sensitivity** | | |
| Band 1 | | |
| 10 Hz to 100 MHz | 25 mVrms | Checked by verifying that counter set to resolution 0 displays a measurement within 1 Hz of the input signal from synthesized signal generator at 25 mVrms. |
| Band 2 | | |
| 100 MHz to 1 GHz | -15 dBm | Checked by verifying that counter set to resolution 0 displays a measurement within 1 Hz of the input signal from synthesized signal generator at -15 dBm. |
| Band 3 | | |
| 0.95 to 12.4 GHz<br>12.4 to 20 GHz | -25 dBm<br>-20 dBm | Checked by verifying that counter displays a reading within 1 Hz of input signal from synthesized signal generator at specified power level. |

Table 8-1. Performance Verification Test Methods. (Continued)

| Counter Characteristic | Performance Specifications | Test Method |
|---|---|---|
| **Maximum Input** | | |
| Band 1 | | |
| 10 Hz to 100 MHz | 1 Vrms | Checked by verifying that the counter performs accurate measurement at maximum power level. |
| Band 2 | | |
| 100 MHz to 1 GHz | +10 dBm | Checked by verifying that the counter performs accurate measurement at maximum power level. |
| Band 3 | | |
| 950 MHz to 20 GHz | +10 dBm | Checked by verifying that the counter performs accurate measurement at maximum power level. |
| **Amplitude Discrimination** | | |
| Band 3 | | |
| 950 MHz to 20 GHz | 10 dB | Checked by verifying that counter measures the higher power signal of two signals input from signal generators. |
| **Center Frequency** | | |
| Band 2 | | |
| 100 MHz to 1 GHz | Counter locks a signal 5 MHz from entered frequency. | Checked by applying a signal 10 MHz from the entered frequency, and verifying that it is not read, and applying a signal 5 MHz from the entered frequency, and verifying that it is read. |

## EQUIPMENT REQUIREMENTS

Equipment required for performing performance tests on the EIP Model 625A counter is listed in Table 8-2.

**NOTE**

Minimum use specifications are the principal parameters required for performance of the procedures and are included to assist in the selection of alternate equipment. Satisfactory performance of alternate items should be verified prior to use. All applicable equipment must bear evidence of current calibration.

**Table 8-2. Recommended Equipment Requirements.**

| Equipment | Range | Recommended Manufacturer | Model |
|---|---|---|---|
| Synthesized Microwave Sweeper (2) | 10 MHz to 26.5 GHz | Hewlett Packard | 8340A |
| Frequency Synthesizer | 100 Hz to 10 MHz | Hewlett Packard | 3325A |
| Sweep Generator | 3 to 18 GHz | Wiltron | 6635B |
| Spectrum Analyzer | 100 Hz to 22 GHz | Hewlett Packard | 8566A |
| Power Meter | 10 MHz to 26.5 GHz | Hewlett Packard | 437B |
| Power Sensor | 10 MHz to 18 GHz | Hewlett Packard | 8481A |
| Power Sensor | 50 MHz to 26.5 GHz | Hewlett Packard | 8485B |
| Oscilloscope | DC to 100 MHz | Tektronix | 475 |
| Power Splitter | 10 MHz to 26.5 GHz | Hewlett Packard | 11667B |
| Directional Coupler | 10 to 1000 MHz | Anzac | CH132 |
| Directional Coupler | 950 MHz to 18 GHz | Narda | 4222-16 |
| Directional Coupler | 18 to 26.5 GHz | Narda | 4017B-10 |
| Bidirectional Coupler | 10 dB | Narda | 3022 |
| Low Attenuation Coaxial Cable (3) | | Gore | P2S01S01036.0 |
| 6 dB Attenuator (2) | DC to 1 GHz | Texscan | FP-50 |
| 3 dB Attenuator (3) | DC to 26.5 GHz | Weinschel | 9-3 |
| Detector | 10 MHz to 18 GHz | Hewlett Packard | 8473B |
| 50 Ohm Termination | | Pamona | 4119-50 |

## TEST PROCEDURES

**NOTE**

Review the entire procedure before starting the verification testing process. Verify that the line voltage selector is properly set for the intended single-phase line voltage. Connect the instrument to local line voltage before starting any test.

### BAND 1 – RANGE AND SENSITIVITY TEST

#### Description

This test verifies counter operation from 10 Hz to 100 MHz at 25 mVrms (70.7 mV p-p). The oscilloscope is used to set signal levels below 10 MHz, and the power meter is used to set signal levels at 10 MHz and above. Test setup 1 tests the counter from 10 Hz to 10 MHz and test setup 2 tests the counter from 20 MHz to 100 MHz.

#### Equipment

Synthesized Function Generator (Wavetek 23)
Sweep Generator (Wiltron 6647B)
Source Locking Counter (EIP 578B)
Power sensor (Hewlett Packard 8481A)
Power splitter (Hewlett Packard 11667B)
Power Splitter (Hewlett Packard 11687B)
Oscilloscope (Tektronix 475)

#### Equipment Setup 1

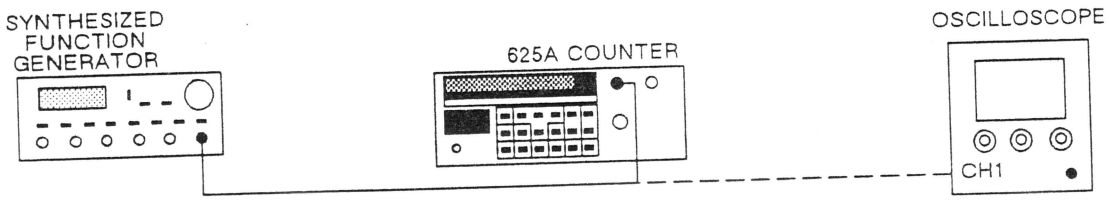



**Figure 8-1. Band 1 Range and Sensitivity Test Setup (10 Hz to 10 MHz).**

#### Procedure

1. Connect equipment as shown in Figure 8-1.
2. Set the counter to Band 1 and select resolution 0 (1 Hz resolution).
3. Set the output frequency from the synthesizer to 10 Hz.
4. Using the oscilloscope, set the output signal level from the synthesizer to 70.7 mV p-p.
5. Apply the signal to the counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz.

**Equipment Setup 2**

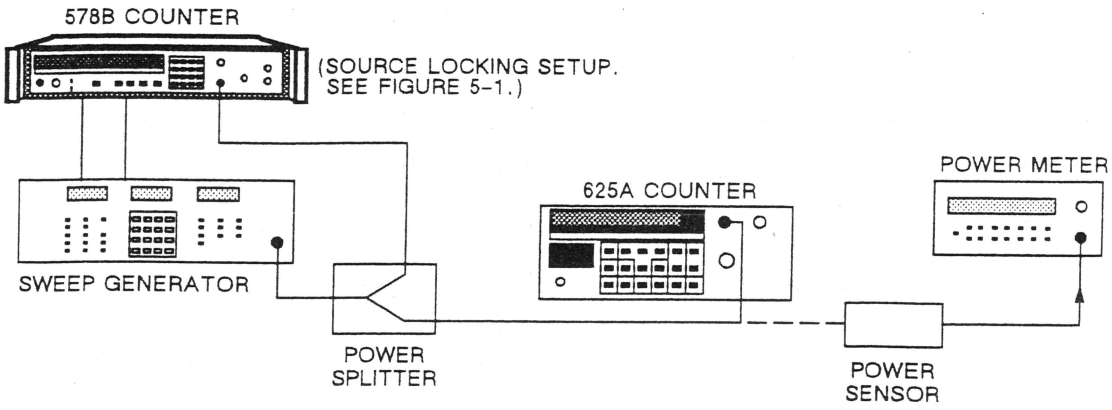



**Figure 8-2. Band 1 Range and Sensitivity Test Setup (20 MHz to 100 MHz).**

**Procedure**

1. Connect equipment as shown in Figure 8-2.
2. Set the 625A counter to Band 1 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 20 MHz.
4. Using the oscilloscope, set the output signal level from the sweeper to 70.7 mV p-p.
5. Apply the signal to the 625A counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 40, 80 and 100 MHz.

## BAND 2 RANGE AND SENSITIVITY TEST

**Description**

This test verifies counter operation from 100 MHz to 1 GHz at -15 dBm.

**Equipment Required**

Synthesized microwave sweeper (Hewlett Packard 8340A)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Power splitter (Hewlett Packard 11667B)

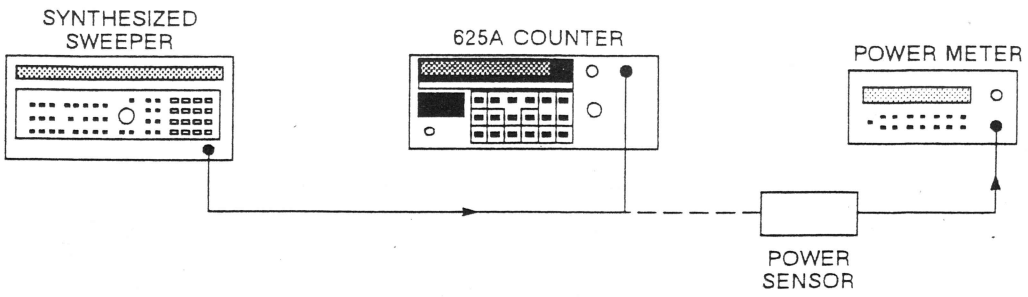



**Figure 8-3. Band 2 Range and Sensitivity Test Setup.**

### Procedure

1. Connect equipment as shown in Figure 8-3.
2. Set 625A counter to Band 2 and select resolution 3.
3. Set synthesizer to 250 MHz.
4. Using power meter, set output signal level from synthesizer to -15 dBm.
5. Apply 250 MHz signal to 625A counter and verify proper reading.
6. Repeat steps 3, 4, and 5 at 300, 400, 500, 600, 700, 800, and 900 MHz and 1 GHz.
7. Repeat steps 3 through 6 at an input power of +7 dBm.

## BAND 3 RANGE AND SENSITIVITY TEST

### Description

This test verifies counter operation from 950 MHz to 20 GHz at -20 dBm and +7 dBm for all CW signals.

### Equipment Required

Synthesized sweeper (Hewlett Packard 8340A)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8485A)
Power splitter (Hewlett Packard 11667B)

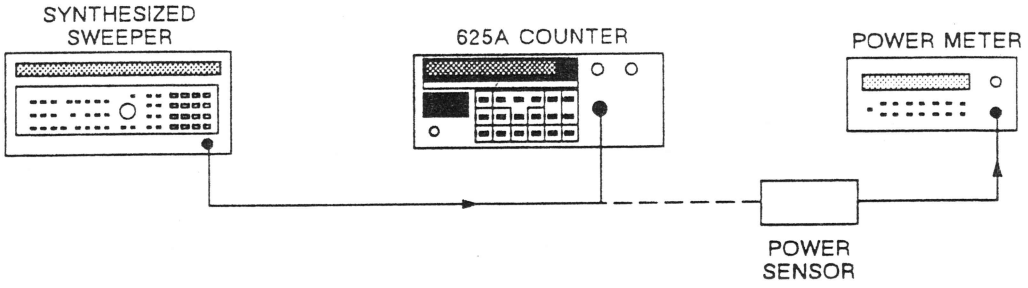



**Figure 8-4. Band 3 Range and Sensitivity Test Setup.**

### Procedure

1. Connect equipment as shown in Figure 8-4.
2. Set 625A counter to Band 3 and select resolution 3.
3. Set synthesizer to 950 MHz.
4. Using power meter, set output signal level from synthesizer to -20 dBm.
5. Apply 950 MHz signal to 625A counter and verify proper reading.
6. Repeat steps 3, 4, and 5 at 1, 3, 6, 10, 12.4, 15, 18, and 20 GHz.
7. Repeat steps 3 through 6 at the input power of +7 dBm.

## BAND 3 AMPLITUDE DISCRIMINATION TEST

### Description

This test verifies that the counter will measure accurately the larger of two signals differing in amplitude by 10 dB or more.

### Equipment Required

Synthesized sweeper (2) (Hewlett Packard 8340A)
Spectrum analyzer (Hewlett Packard 8566A)
Power splitter (Hewlett Packard 11667B)

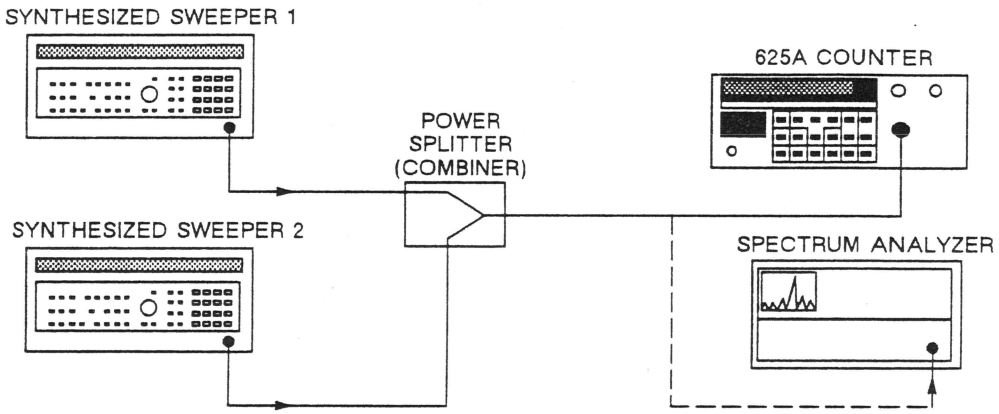



**Figure 8-5. Band 3 Amplitude Discrimination Test Setup.**

### Procedure

1. Connect equipment as shown in Figure 8-5.
2. Set synthesized sweeper 1 to 3 GHz at 0 dBm and set synthesized sweeper 2 to 3.1 GHz at -15 dBm.
3. Verify that 625A counter correctly measures the frequency of the high power signal source.
4. Repeat steps 2 and 3 at 6, 6.1, 12,12.1, 18, and 18.1 GHz.

## BAND 3 CENTER FREQUENCY TEST

### Description

This test verifies that the counter locks on a signal +50 MHz from the center frequency.

### Equipment Required

Synthesized sweeper (Hewlett Packard 8340A)
Low attenuation coaxial cable (Gore P2S01S01036.0)

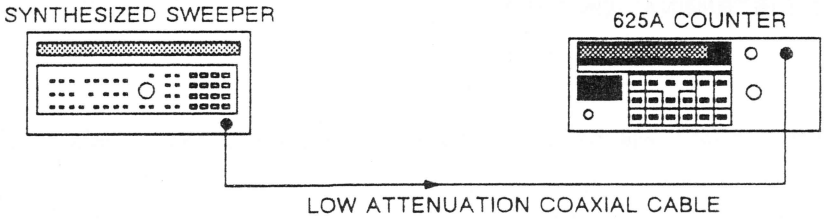



**Figure 8-6. Band 2 Center Frequency Test Setup.**

**Procedure**

1. Connect equipment as shown in Figure 8-6 and turn equipment on.
2. Set 625A counter to Band 3 and press keys for CENTER FREQUENCY 3 GHz.
3. Set sweeper to center frequency minus 50 MHz. Set power level to sensitivity level. Verify that reading on counter display is accurate.
4. Set sweeper to center frequency plus 50 MHz. Verify that reading on counter display is accurate.

# SECTION 9
# TROUBLESHOOTING

## INTRODUCTION

This section defines troubleshooting aids that can be used to identify malfunctions within the 625A counter. They are:

1. Self diagnostics
2. Keyboard-controlled circuit tests
3. Troubleshooting trees

The procedures and tables provided in this section are for troubleshooting to a functional circuit level.

## SELF DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests, it then enters the normal operating mode. If the counter fails any checks, an error number is displayed. Refer to error message listing at the end of section 3 to determine cause of error.

## KEYBOARD-CONTROLLED CIRCUIT TESTS

There are six keyboard-controlled circuit tests (01 through 06) which are accessed by pressing SPECIAL FUNC and the two-digit test number. These tests do not require keyboard inputs to function, and all except 05 can be exited by pressing any key. Test 05, which uses the keyboard in its operation, is exited by pressing CLEAR DISPLAY. This causes the counter to return to normal operation.

01 **100 MHz Self Test.** This function verifies operation of the count chain, gate generator, and VCO. The display shows 100 MHz $\pm$1 count. These results are output to the GPIB interface when frequency readings are requested.

02 **Light Display Segments Test.** This function verifies that all digit segments and annunciator LEDs are operational. When this function is activated, all digit segments and all annunciators are turned on.

03 **Scan Display Segments Test.** Each segment in all the digits and the bank of annunciators is turned on sequentially by this function to test the display segment drivers. The scan rate is determined by the setting of the SAMPLE RATE up and down controls. For manual control, activate sample rate hold, and press the "." key to activate a single segment.

04 **Scan Display Digits Test.** Each digit and each bank of annunciators is turned on sequentially by this function to check the display digit driver. The scan rate is determined by the setting of the SAMPLE RATE up and down controls. For manual control, activate sample rate hold, and press the "." key to activate a single digit or annunciator.

05 **Keyboard Test.** This function verifies the operation of the keyboard. When this function is activated, the counter stops normal operation, and the display shows the key code of the last key pressed. (See table on following page.) When a new key is pressed, the display is updated to show the code of the new key. The CLEAR DISPLAY key will not return a key code, but will instead return the counter to normal operation. When the GPIB controller requests a key code, the code

of the last key pressed is output. If the controller requests a key code, the counter outputs to the GPIB interface the code of the last key pressed even if Special Function 05 is not activated. If the counter is in local, this function must be terminated by the CLEAR DISPLAY key. If it is in remote, this function can be terminated by any device-dependent command.

| Key | Code |
|---|---|
| SPECIAL FUNC | 35 |
| BAND | 36 |
| 0/RESET LOCAL | 31 |
| 7/SAMPLE RATE up | 12 |
| 4/FREQ offset | 22 |
| 1 | 32 |
| 8/SAMPLE RATE hold | 13 |
| 5/CENTER FREQ | 23 |
| 2 | 33 |
| 9/SAMPLE RATE down | 14 |
| 6/FREQ mult | 24 |
| 3 | 34 |
| GHz | 15 |
| MHz | 25 |
| "." (decimal or trigger) | 21 |
| CLEAR DATA | 16 |
| CLEAR DISPLAY | exits test |
| RESOL | 11 |

06 **PROM Check Sum Test.** This function generates the check sum for the PROM in the counter and compares it with the check sum stored in the firmware. If the check sum generated is correct, the counter displays the word "PASSEd" on the front panel. If the check sum is incorrect, an error message is output to the display. At the same time, the ERROR CONDITION status bit in the GPIB serial poll status byte is set. During check sum generation, "SPECIAL 06" is displayed.

## TROUBLESHOOTING TREES

The following troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any PC boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A1 Motherboard
- A2 Power Supply
- A5 Processor/GPIB
- A6 Count Chain/Gate
- A9 Signal Conditioner

### CAUTION

**Do not attempt to repair or disassemble the A10 hybrid assembly.**

## TEST EQUIPMENT REQUIRED

**Table 9-1. Troubleshooting Test Equipment.**

| Equipment | Range | Recommended Manufacturer | Model |
|---|---|---|---|
| Synthesized Sweeper | 10 MHz to 26.5 GHz | Hewlett Packard | 8340A |
| Frequency Synthesizer | 100 Hz to 10 MHz | Hewlett Packard | 3325A |
| Spectrum Analyzer | 100 Hz to 22 GHz | Hewlett Packard | 8566A |
| Power Meter | 10 MHz to 26.5 GHz | Hewlett Packard | 437B |
| Power Sensor | 10 MHz to 18 GHz | Hewlett Packard | 8481A |
| Power Sensor | 50 MHz to 26.5 GHz | Hewlett Packard | 8485B |
| Oscilloscope | DC to 130 MHz | Tektronix | 475 |
| Oscilloscope Voltage Probe | DC to 3.5 GHz | Tektronix | P6056 |
| Power Splitter | 10 MHz to 26.5 GHz | Hewlett Packard | 11667B |
| Directional Coupler | 10 to 1000 MHz | Anzac | CH132 |
| Directional Coupler | 950 MHz to 18 GHz | Narda | 4222-16 |
| Directional Coupler | 18 to 26.5 GHz | Narda | 4017B-10 |
| Low Attenuation Coaxial Cable (3) | | Gore | P2S01S01036.0 |
| 6 dB Attenuator (2) | DC to 1 GHz | Texscan | FP-50 |
| 3 dB Attenuator (3) | DC to 26.5 GHz | Weinschel | 9-3 |
| Detector | 10 MHz to 18 GHz | Hewlett Packard | 8473B |
| 50 Ohm Termination | | Pamona | 4119-50 |

Before servicing any unit, verify that:

1. The line voltage and fuse are correct for the voltage setting.
2. Special Function 09 is selected (internal 10 MHz time base). If Special Function 08 is selected (external 10 MHz time base), check that a 10 MHz reference signal is applied to the 10 MHz IN/OUT connector on the rear panel.

To use the troubleshooting trees.

1. Refer to the main troubleshooting tree.
2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.
3. Refer to the appropriate troubleshooting tree for that failure mode.

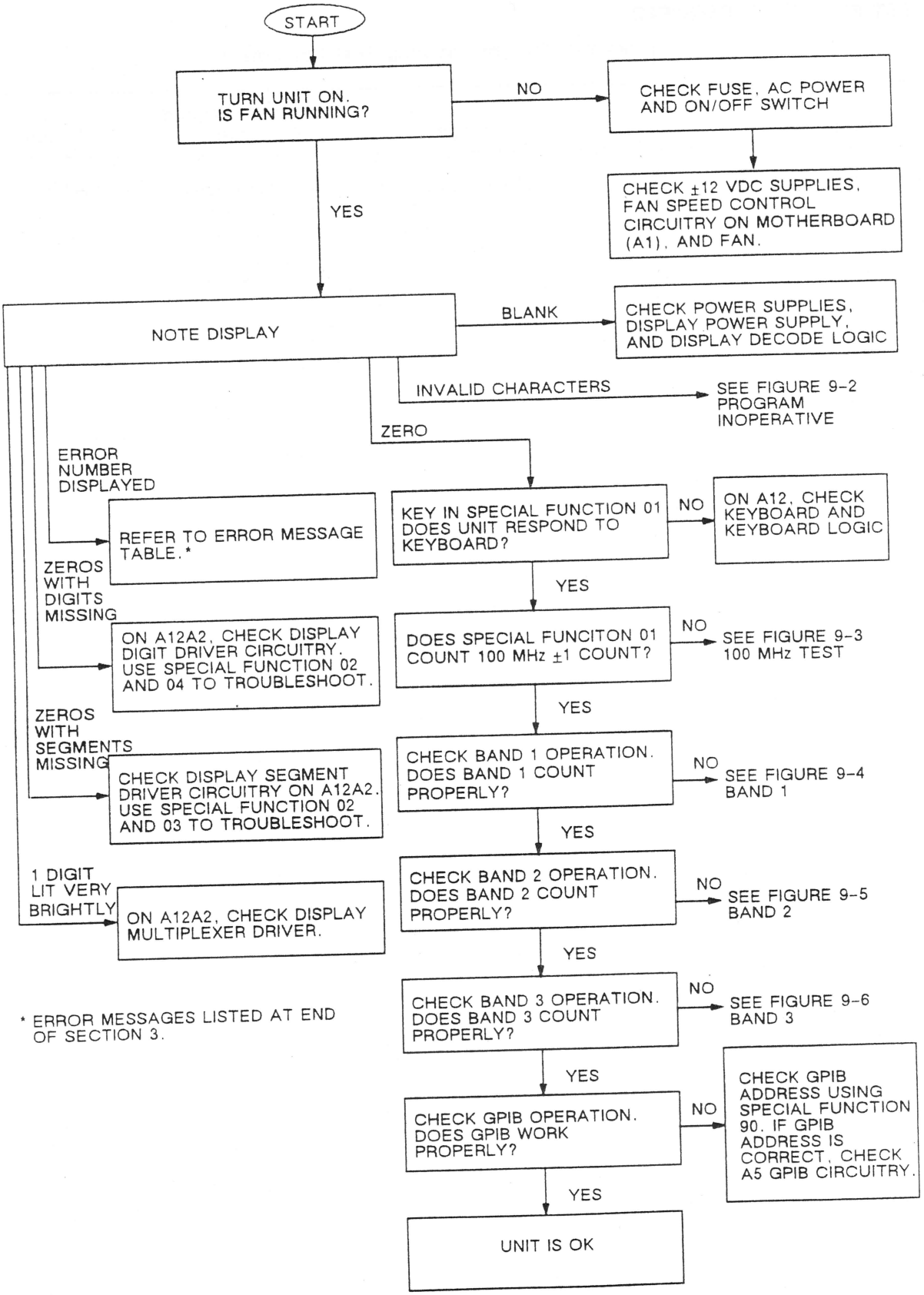



**Figure 9-1. Main Troubleshooting Tree.**

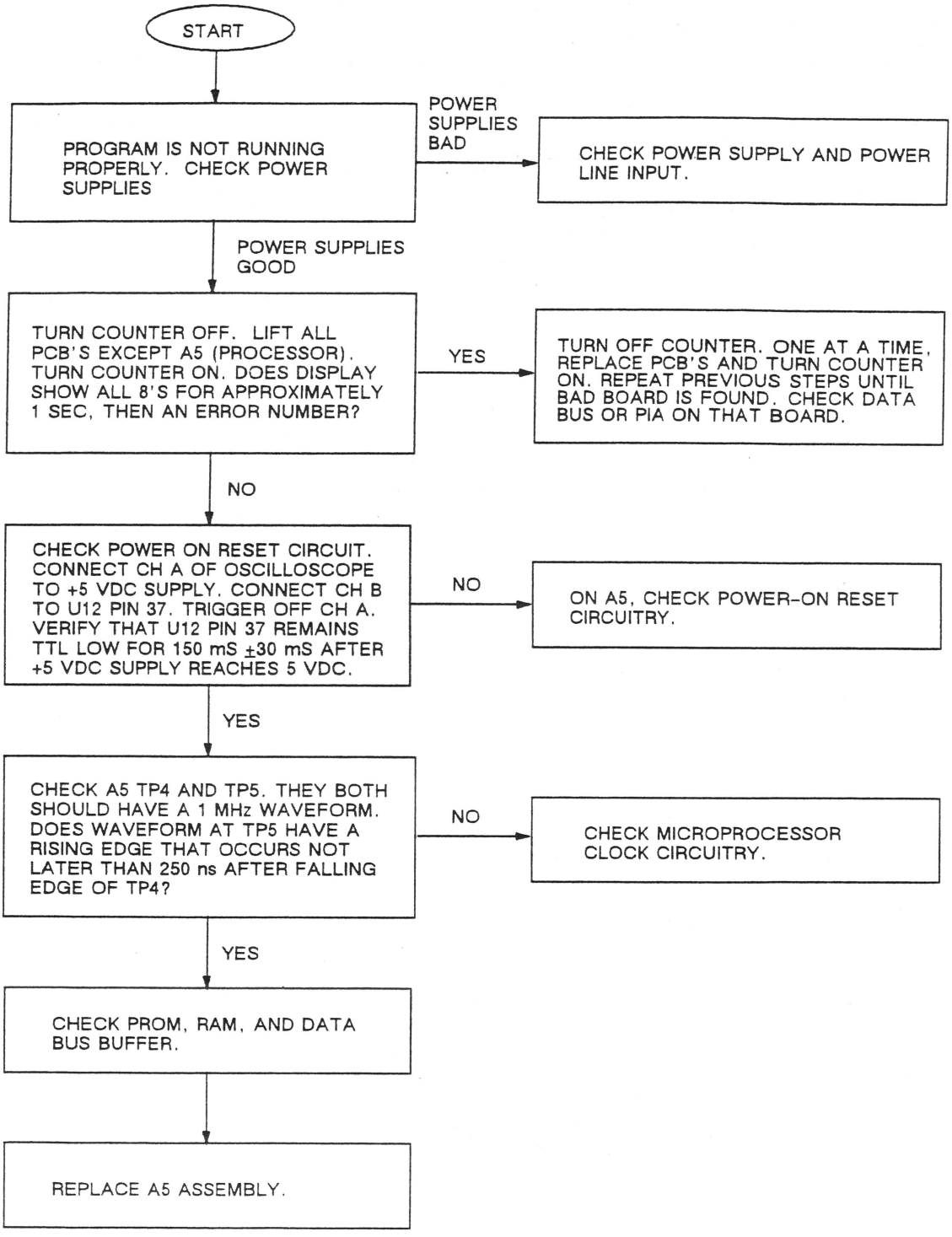



Figure 9-2. Program Inoperative Troubleshooting Tree.

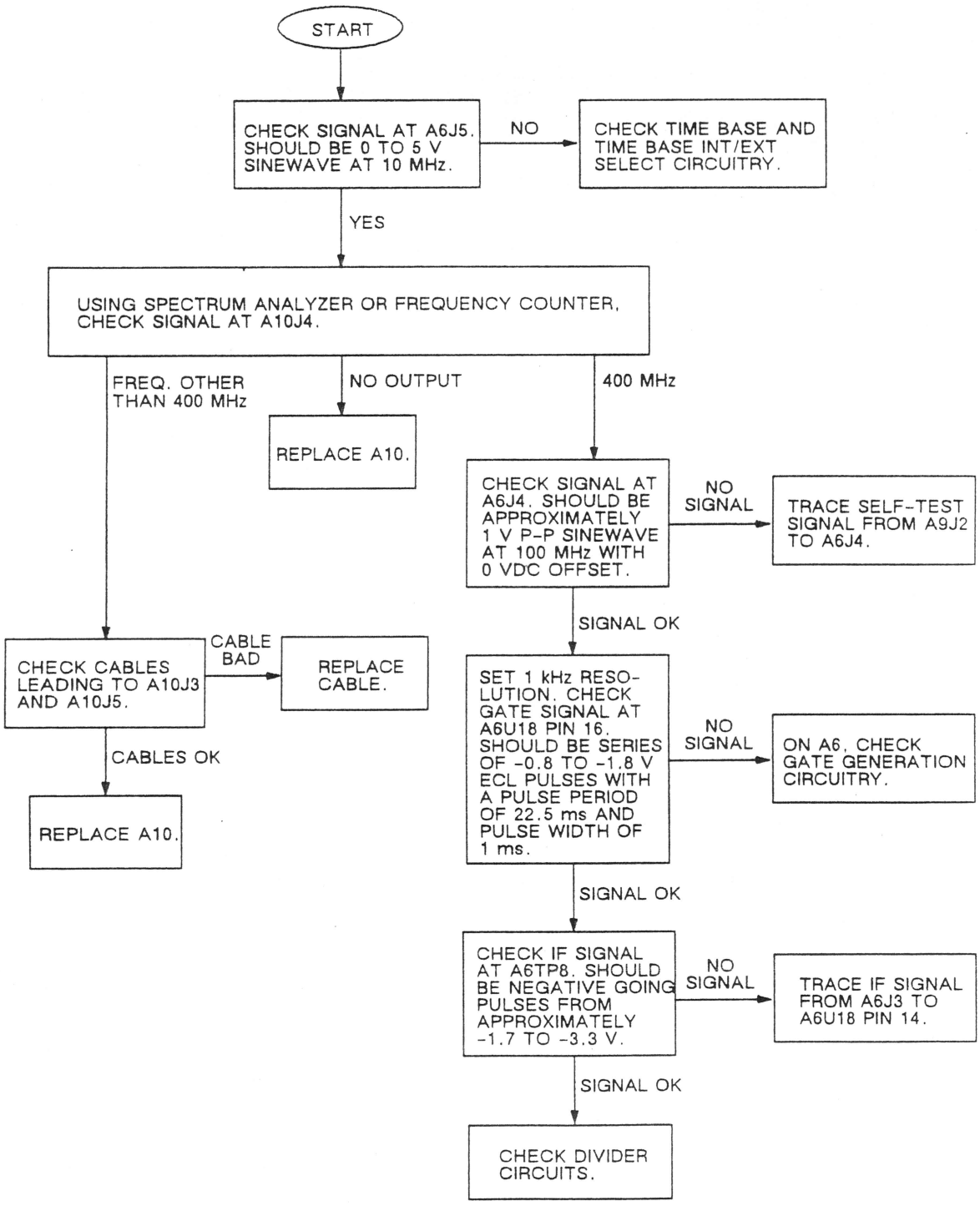



**Figure 9-3. 100 MHz Self-Test Troubleshooting Tree.**

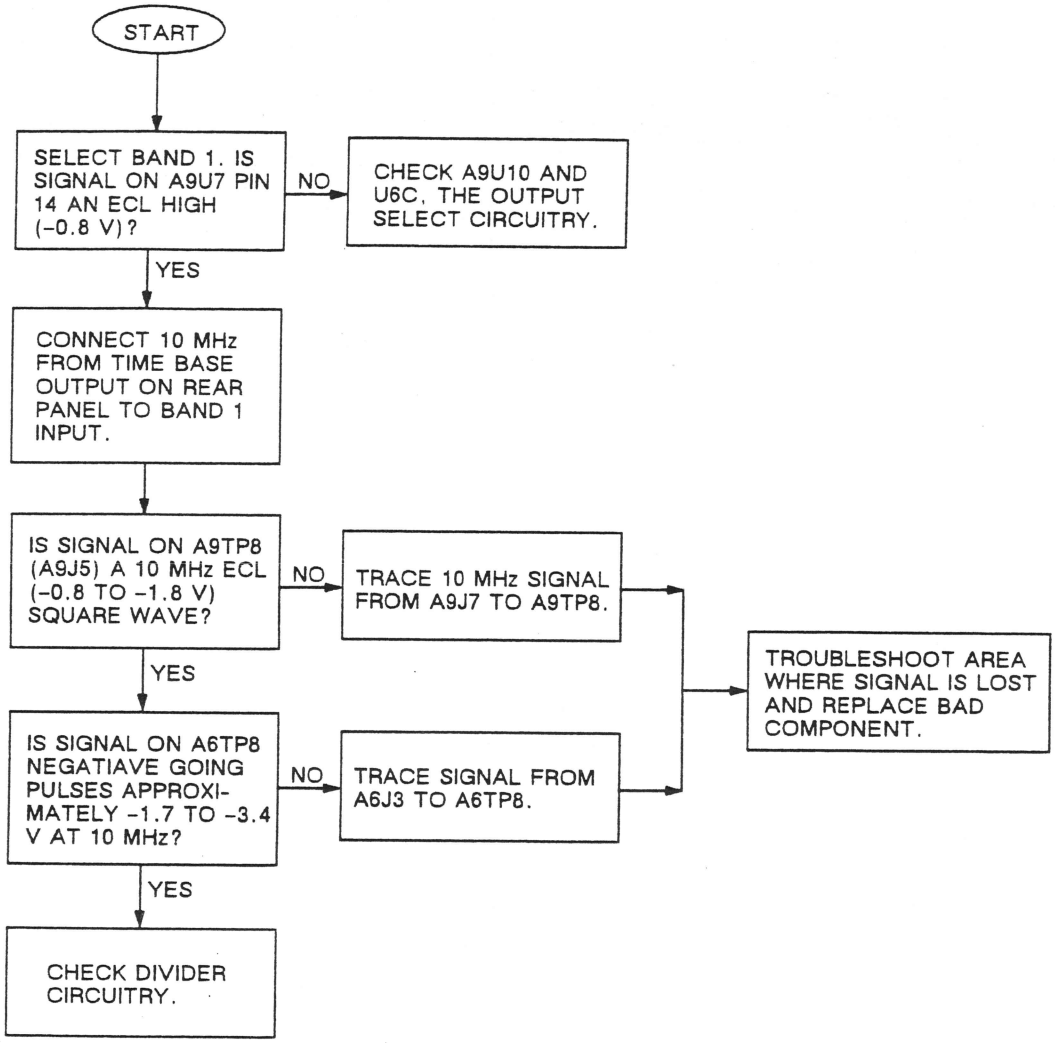



**Figure 9-4. Band 1 Troubleshooting Tree.**

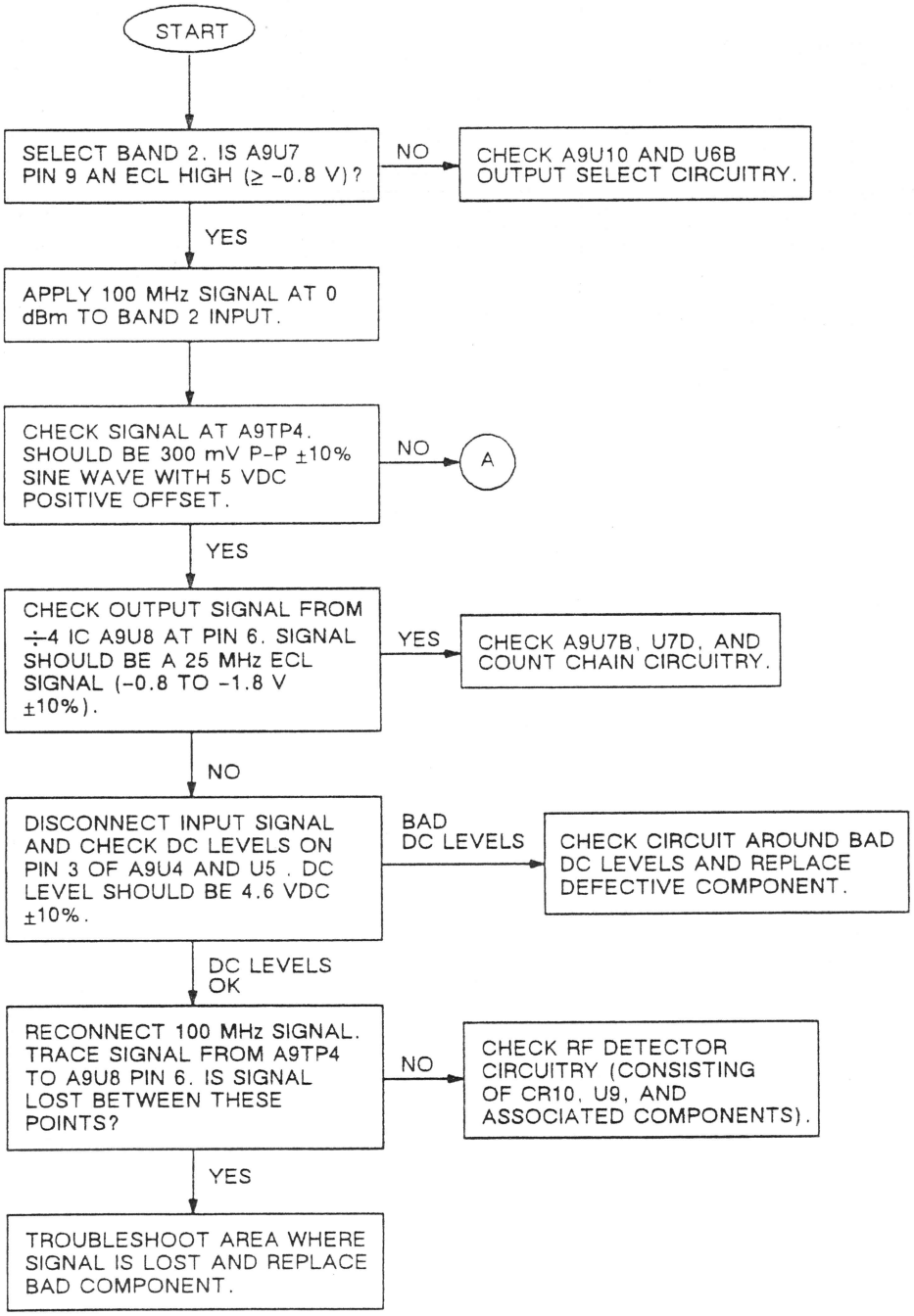



Figure 9-5. Band 2 Troubleshooting Tree.
(Sheet 1 of 2)

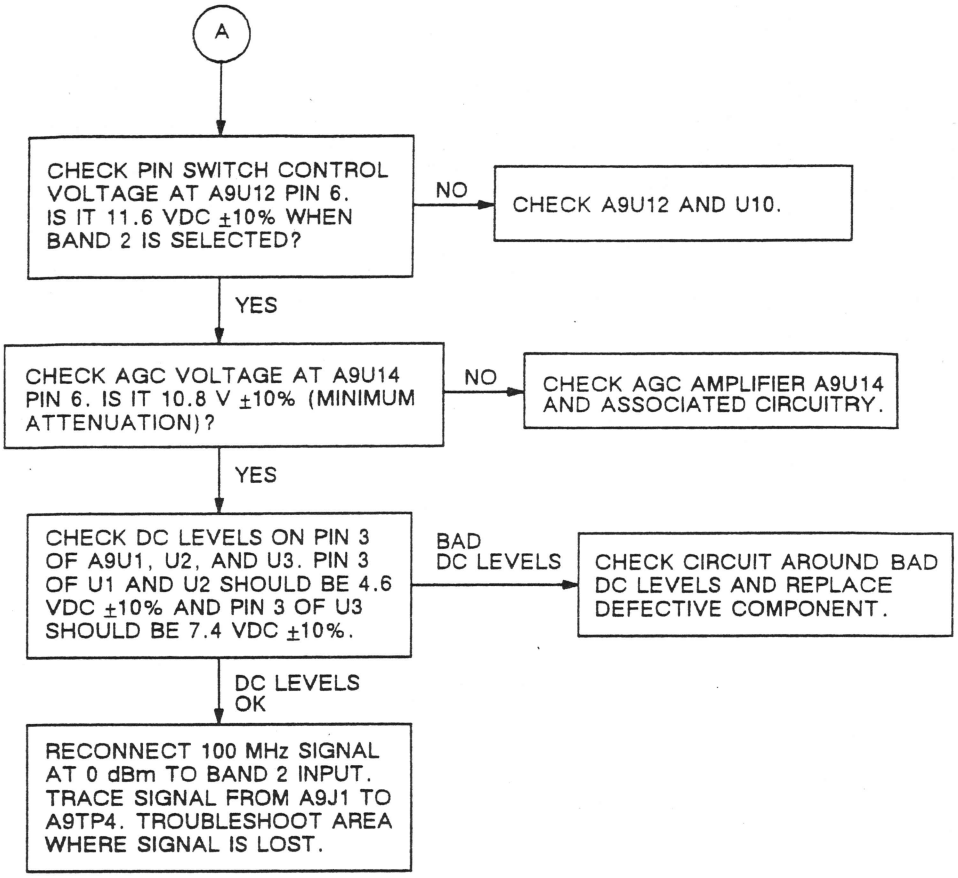



**Figure 9-5. Band 2 Troubleshooting Tree. (Sheet 2 of 2)**

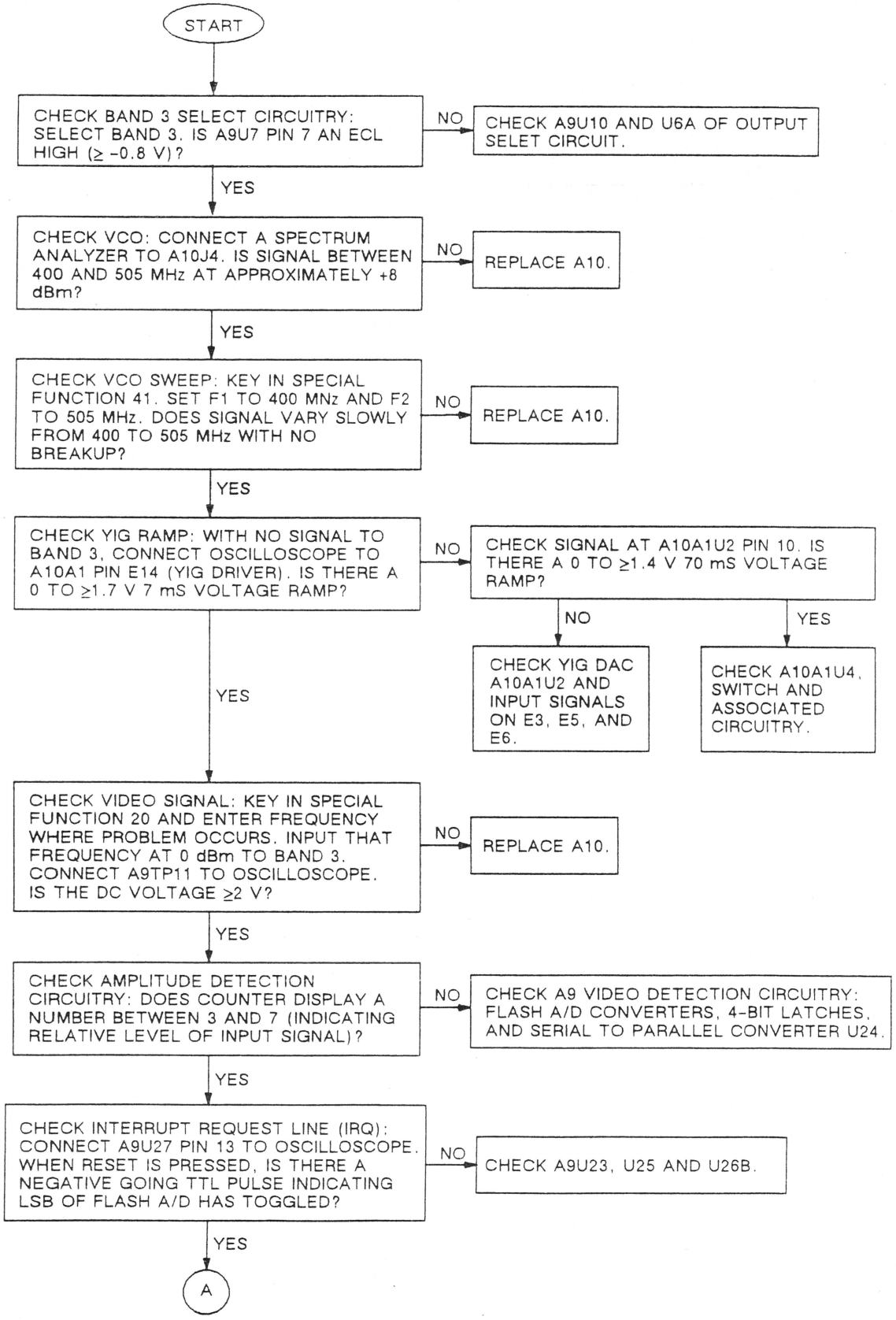



**Figure 9-6. Band 3 Troubleshooting Tree.**
**(Sheet 1 of 2)**

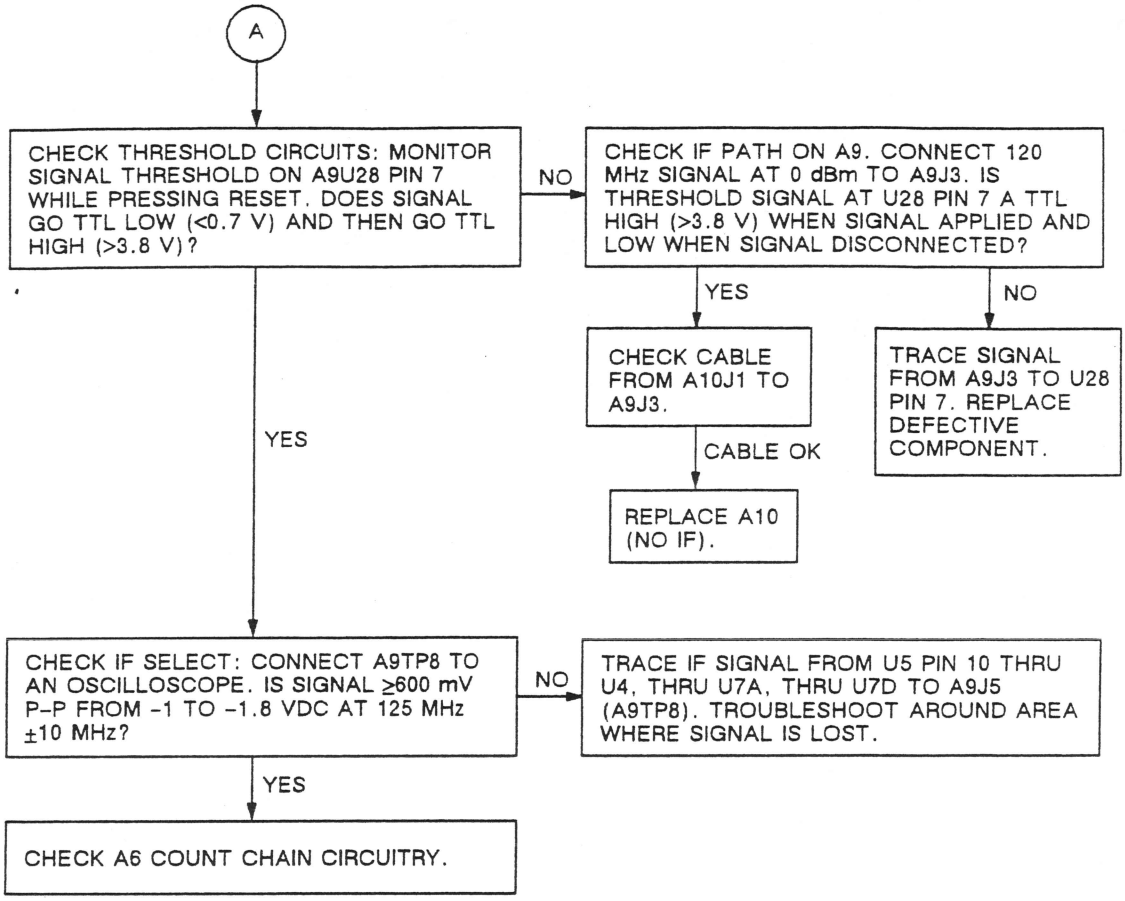



**Figure 9-6. Band 3 Troubleshooting Tree.**
**(Sheet 2 of 2)**

# SECTION 10
# FUNCTIONAL DESCRIPTIONS AND REPLACEABLE PARTS

## INTRODUCTION

This section contains functional descriptions, lists of replaceable parts, illustrations of component locations, and schematic diagrams for each assembly used in this counter.

The replaceable parts list for electrical assemblies (PCBs) lists the electrical components in alphanumerical order by reference designation. Components having different reference designators but having the same EIP part number are described for the first such component listed. Subsequent descriptions of that component refer to the first entry. The total number of like components used on the same assembly is listed with the first entry in the UNITS PER ASSY column.

The replaceable parts lists for mechanical assemblies is organized according to the item number sequence.

Similar functional descriptions and lists of replaceable parts for the available options are contained in Section 11, Options.

## ORDERING INFORMATION

To order a replaceable part, quote the EIP part number, indicate the quantity required, and address the order to:

EIP Microwave, Inc.
Customer Support
1589 Centre Pointe Drive
Milpitas, CA 95035

To order a part that is not shown on the replaceable parts list, include the instrument model number, serial number, description and function of the part, and the number of parts required. Mail the order to the above address.

## REFERENCE DESIGNATORS

| | |
|---|---|
| A | assembly |
| B | battery or fan |
| C | capacitor |
| CR | diode |
| DS | indicator (display) |
| F | fuse |
| J | jack |
| K | relay |
| L | inductor |
| P | plug |
| Q | transistor |
| R | resistor |
| RN | resistor network |
| S | switch |
| T | transformer |
| TP | test point |
| U | integrated circuit |
| W | wire or cable |
| X | socket or holder |
| Y | crystal, piezoelectric |

## ABBREVIATIONS

| | |
|---|---|
| A | ampere, assembly |
| ac | alternating current |
| A/D | analog-to-digital (converter) |
| ADJ | adjustable |
| AMP | amplifier |
| ASSY | assembly |
| ATTEN | attenuator |
| BCD | binary coded decimal |
| BLK | black |
| CAP | capacitor |
| CC | carbon composition |
| CER | ceramic |
| CLK | clock |
| CMOS | complimentary metal oxide semiconductor |
| CNTR | counter |
| COAX | coaxial |
| COM | common |
| CONN | connector |
| CONV | converter |

## ABBREVIATIONS (Continued)

| | |
|---|---|
| COR | corner |
| CRES | corrosive resistant steel |
| CW | continuous wave |
| dB | deciBel |
| DAC | digital-to-analog converter |
| dc | direct current |
| DEC | decade |
| DEG | degree |
| DET | detector |
| DIA | diameter |
| DIFF | differential |
| DIP | dual inline package |
| DIV | divider |
| ECL | emitter-coupled logic |
| EEPROM | electrically erasable programmable memory |
| ELECTLT | electrolytic |
| EXCL | exclusive |
| EXT | external |
| FF | flip-flop |
| FR | front |
| FREQ | frequency |
| FRICTLK | friction lock |
| GHz | gigahertz ($10^9$ hertz) |
| GP | general purpose |
| GPIB | general purpose interface bus |
| GRN | green |
| GRY | gray |
| H | henry (inductance) |
| HARN | harness |
| HDR | header |
| HEX | hexadecimal, hexagon |
| HI SP | high speed |
| IC | integrated circuit |
| IF | intermediate frequency |
| INSUL | insulated |
| INTCON | interconnection |
| INTFC | interface |
| INTL | internal |
| I/O | input/output |
| K | kilo |
| kHz | kilohertz ($10^3$ hertz) |
| LED | light emitting diode |
| LG | large |
| LO | local oscillator |
| LPF | low pass filter |
| LSB | least significant bit (byte) |
| LSD | least signicicant digit |
| MHz | megahertz ($10^6$ hertz) |
| µF | microfarad |
| MF | metallic film |
| µH | microhenry |
| µP | microprocessor |
| µs | microsecond |
| ML | mylar |
| MOD | model |
| MOM | momentary |
| MOS | metal oxide semiconductor |
| M/OX | metal oxide |
| MP | microprocessor |
| MS | monostable |
| MTG | mounting |
| MUX | multiplexer |
| NEG | negative |
| NPN | negative-positive-negative (transistor) |
| NPO | temperataure coefficient (capacitors) |
| NTWK | network |
| ns | nanosecond |
| O.D. | outside diameter |
| OCXO | oven controlled crystal oscillator |
| OSC | oscillator |
| PAL | programmable array logic |
| PC | printed circuit |
| PCB | printed circuit board |
| pF | picofarad |
| PIA | peripheral interface adapter |
| PIN | positive intrinsic negative (diode) |
| PLL | phase locked loop |
| PNP | positive-negative-positive (transistor) |
| PNH | panhead |
| POT | potentiometer |
| prgm | program/programmable |
| PRF | pulse repetition frequency |
| PRL | parallel |
| PROM | programmable read only memory |
| PRPHL | peripheral |
| PSVT | passivated |
| RAM | random access memory |
| RCPT | receptacle |
| RCVR | receiver |
| RECT | rectifier |
| REF | reference |
| REG | regulator (see also RGLTR) |
| RES | resistor |
| RF | radio frequency |
| RGLTR | regulator (see also REG) |
| RN | resistor network |
| R/W | read/write |
| SB | slow blow (fuse) |
| SCR | screw |
| SEG | segment |
| SEMS | screw/washer combination |
| SER/PAR | serial-to-parallel |
| SFLKG | self locking |
| SMD | surface mounted device |
| SPDT | single pole double throw |
| SR | serial |
| SQ | square |
| SRC | semirigid coax |
| SW | switch |
| TANT | tantalum |
| TCXO | temperature compensated crystal oscillator |
| TP | test point |
| TPL | triple |
| TTL | transistor-transistor logic |
| UHF | ultrahigh frequency |
| UNC | unified coarse thread |
| UV | ultraviolet |
| V | volts |
| VCO | voltage controlled oscillator |
| VAC | volts ac |
| Vdc or VDC | volts dc |
| VHF | very high frequency |
| Vrms | voltage root-mean-square |
| W | wire, watt |
| W/ | with |
| W/MNT | with mount |
| W/O | without |
| XCVR | transciever |
| XFMR | transformer |
| X-REC | cross-reces (screw head) |
| XSTR | transistor |
| XTAL | crystal |
| X7R | temperature coefficient (capacitor) |
| YIG | yttrium-iron-garnet |

## TOP ASSEMBLY 2000080-04 Rev. B

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | PANEL ASSY,FRONT,625A | 2010829-02 | 1 |
| 2 | PANEL ASSY,REAR | 2010828-02 | 1 |
| 3 | XMFR ASSY,PWR | 2010832-01 | 1 |
| 4 | FRAME | 5210835-00 | 2 |
| 5 | CARD CAGE ASSY | 2010824-02 | 1 |
| 6 | PCB ASSY,MOTHERBOARD | 2020418-04 | 1 |
| 7 | PROM,PROGRAMMED,625A,PROCESSOR | 2060059-01 | 1 |
| 8 | POST,COR,FR,GRAY,2.70 | 5210430-12 | 2 |
| 9 | POST,CORNER,REAR | 5210863-01 | 2 |
| 10 | PANEL SIDE | 5210854-02 | 1 |
| 11 | PANEL SIDE,VENTED | 5210855-02 | 1 |
| 12 | SCR,PNH X-REC SLFLKG 4-40X5/16 UNC | 5124004-05 | 8 |
| 13 | SCR,PNH X-REC SLFLKG 6-32X3/8 UNC | 5124006-06 | 16 |
| 14 | SCR,PNH X-REC SLFLKG 8-32X1/2 UNC | 5124008-08 | 16 |
| 15 | SCR,FLH,X-REC 100DEG 6-32X5/16 UNC | 5140006-05 | 24 |
| 16 | SCR,PNH,X-REC,SEMS,INTL,4-40X3/8 | 5171004-06 | 1 |
| 17 | NUT,HEX,SLFLKG,CRES 4-40 UNC-3B | 5184004-40 | 1 |
| 18 | SCR,PNH X-REC SLFLKG 6-32X5/8 UNC | 5124006-10 | 2 |
| 19 | STANDOFF,1/4 HEX,6-32 X 2.590 LG | 5100106-00 | 3 |
| 20 | SCR,PNH X-REC SLFLKG 6-32X1/2 UNC | 5124006-08 | 3 |
| 21 | PCB ASSY,POWER SUPPLY | 2020417-04 | 1 |
| 22 | PCB ASSY,PROCESSOR,SER/PAR | 2020416-01 | 1 |
| 23 | PCB ASSY,COUNT CHAIN/GATE | 2020421-03 | 1 |
| 24 | CONVERTER ASSY,B3 | 2010864-01 | 1 |
| 25 | CABLE ASSY,FLAT RBN,F/P LOGIC | 2040169-01 | 1 |
| 26 | TIE,CABLE 0-4.00 ID | 5000266-00 | 1 |
| 27 | LABEL SET,PCB | 5560287-01 | 1 |
| 28 | COMPOUND,THERMAL | 5602004-00 | 1 |
| 29 | WASHER,FINISHING,.635ID | 5210382-02 | 1 |
| 30 | SCR,PNH X-REC SLFLKG 6-32X1/4 UNC | 5124006-04 | 6 |
| 31 | SCR,PNH X-REC SLFLKG 8-32X3/8 UNC | 5124008-06 | 1 |
| 32 | WASHER,FLAT,CRES NO.8 | 5160008-00 | 1 |
| 33 | PCB ASSY,SIGNAL CONDITIONER | 2020420-03 | 1 |
| 34 | CABLE ASSY,COAX,W9 | 2040475-01 | 1 |
| 35 | CABLE ASSY,COAX,W8 | 2040457-01 | 1 |
| 36 | CABLE ASSY,COAX,W7 | 2040486-01 | 1 |
| 37 | CABLE ASSY,COAX,W3 | 2040455-01 | 1 |
| 38 | CABLE ASSY,COAX,W10 | 2040473-01 | 1 |
| 39 | COVER ASSY,TOP | 2010886-01 | 1 |
| 40 | COVER ASSY,BOTTOM | 2010826-01 | 1 |
| 41 | LABEL, SER.NO. | 5560165-00 | 1 |
| 42 | LABEL,CALIBRATION | 5560180-00 | 1 |
| 43 | LABEL,OPTIONS | 5560181-00 | 1 |
| 44 | HANDLE,FLAT,FLEXIBLE | 5250035-00 | 1 |
| 45 | HANDLE ASSY,REMOVABLE,D GRAY,3.50 | 2010402-12 | 2 |
| 46 | GROMMET,CATERPILLAR,1/16" | 5000355-00 | 3 |
| 47 | BUTTON,PLUG,SS-51034 | 5000246-02 | 2 |
| 48 | FOOT,MOLDED,DP GRAY | 5220003-02 | 4 |
| 49 | PAD, RUBBER, FOOT | 5220002-00 | 4 |
| 50 | SCR,SLFLKG, FOOT 8-18X3/8 | 5000095-00 | 8 |
| | CORD,LINE 3-COND | 5440002-00 | 1 |
| | MANUAL ASSY,625A,OPERATION | 5585043-00 | 1 |

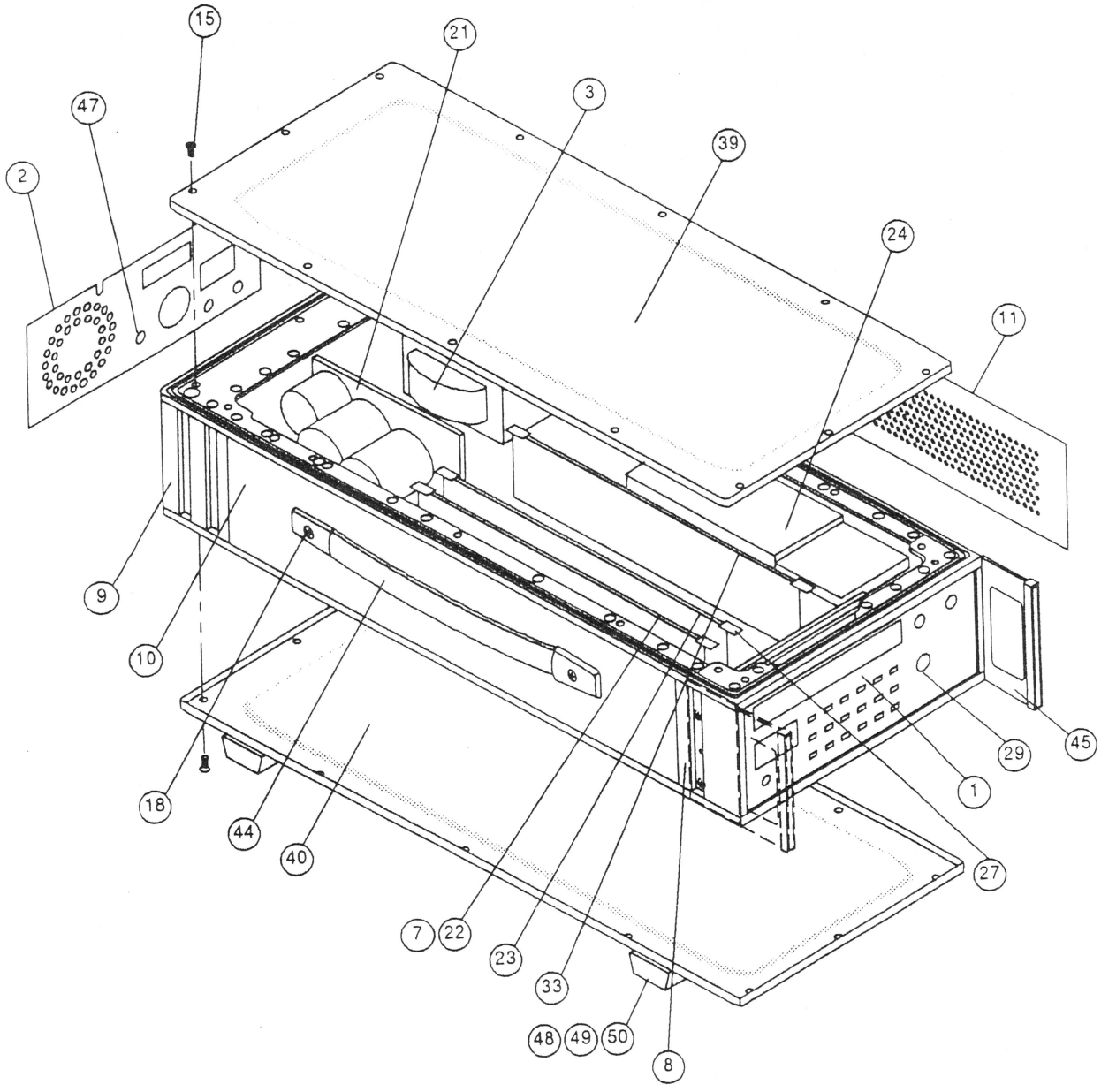



Figure 10-1. Top Assembly, Exploded View.

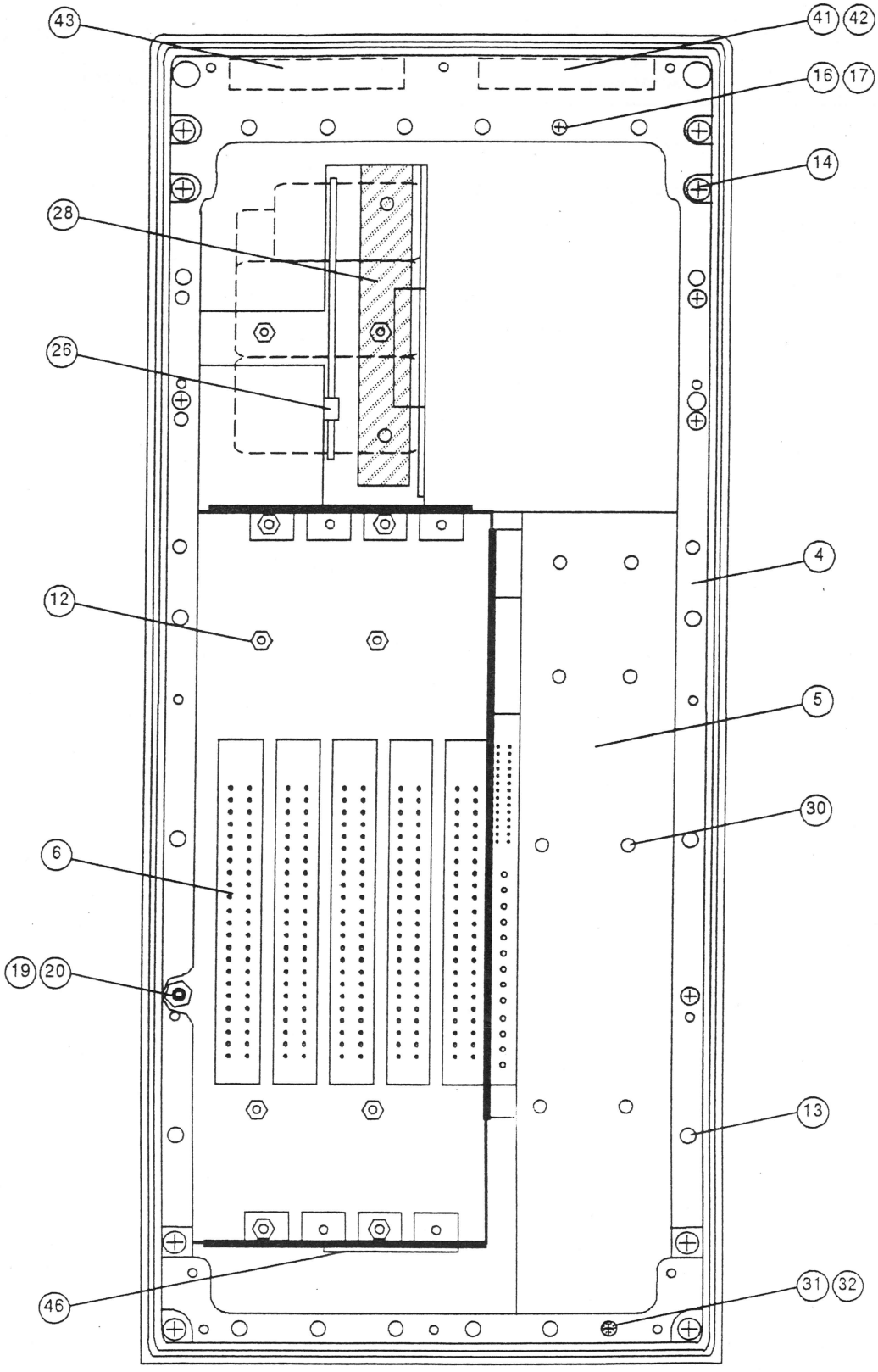



Figure 10-2. Top Assembly, Top View.

Table 10-1. Cable Identification Guide.

| From | Reference Designator | To | Description |
|---|---|---|---|
| A16 | W1 | A2J1 | Transformer Secondary |
| A16 | W2 | W5P1 | Transformer Primary |
| A10J2 | W3 | A9J6 | Video |
| Rear Panel | W4 | A1J7 | Fan |
| Rear Panel | W5 | A16T1P1 | Power Line Voltage Select |
| Rear Panel | W6 | A1J2 | GPIB |
| A10J3 | W7 | A9J2 | VCO |
| A10J1 | W8 | A9J3 | Band 3 IF |
| A6J3 | W9 | A9J5 | IF |
| A10J5 | W10 | A6J5 | 10 MHz |
| A10 | W11 | A1J5 | Band 3 Power and Control |
| A12P1 | W13 | A1J1 | Front Panel Display |
| Front Panel | A12W4 | A9J1 | Band 2 Input |
| Front Panel | A12W6 | A9J7 | Band 1 Input |
| Front Panel | A12W16 | A1J6 | Power On/Off |
| Rear Panel | A12W6 | A6J2 | 10 MHz In/Out |
| Rear Panel | A13W7 | Frame | Safety Ground |

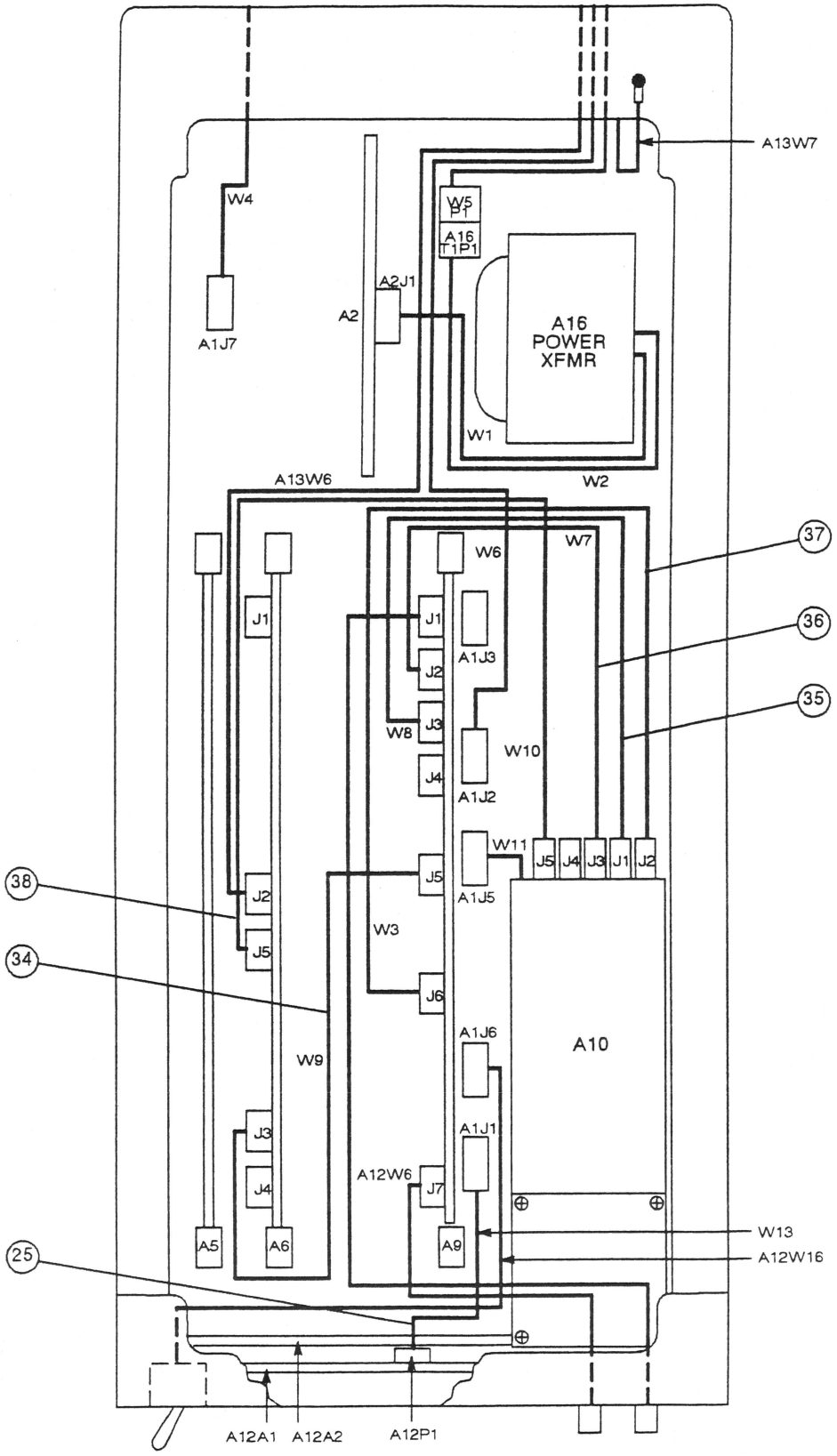



Figure 10-3. Counter Cable Assemblies.

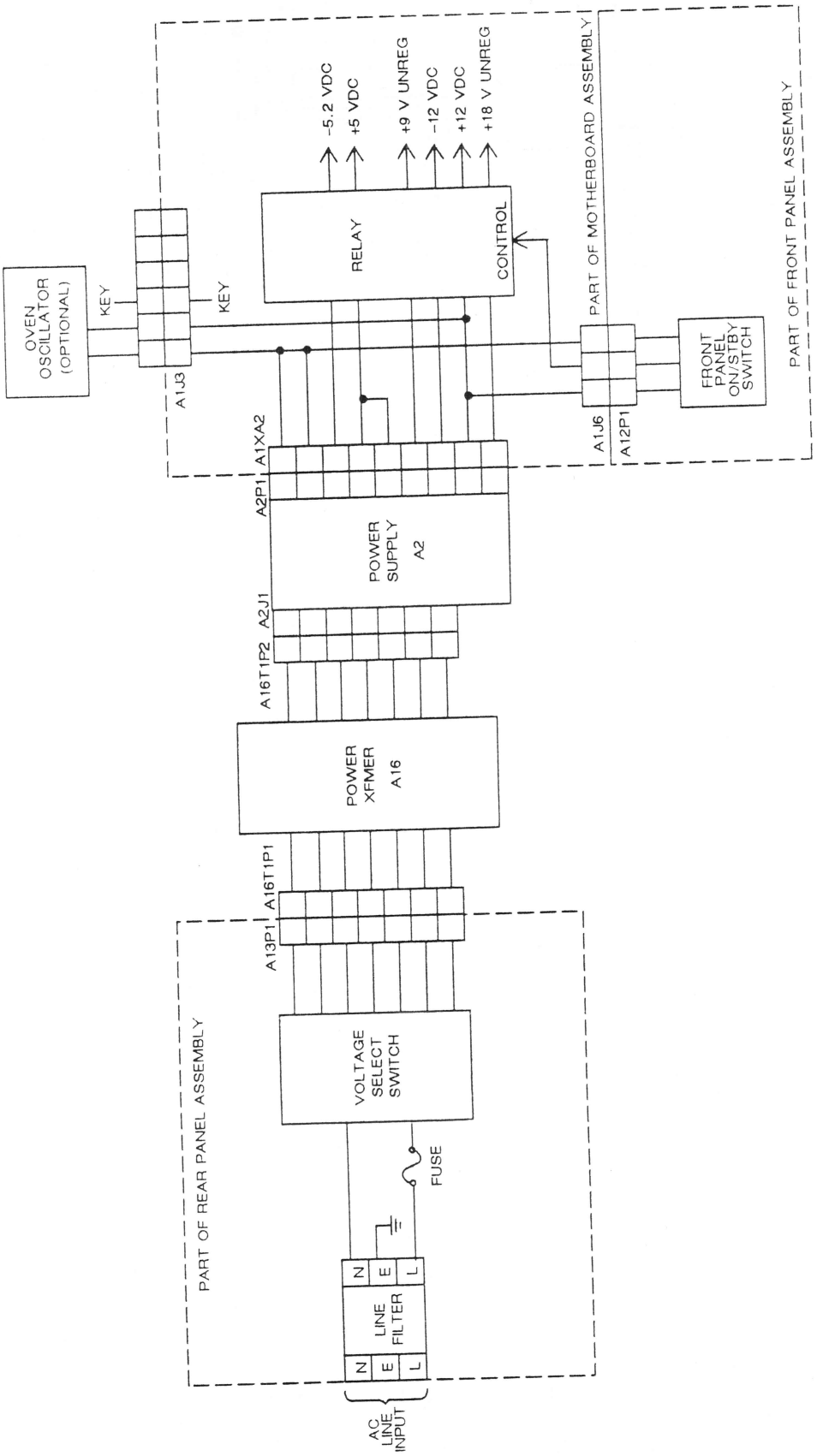



Figure 10-4. Power Entry Interconnect Diagram.

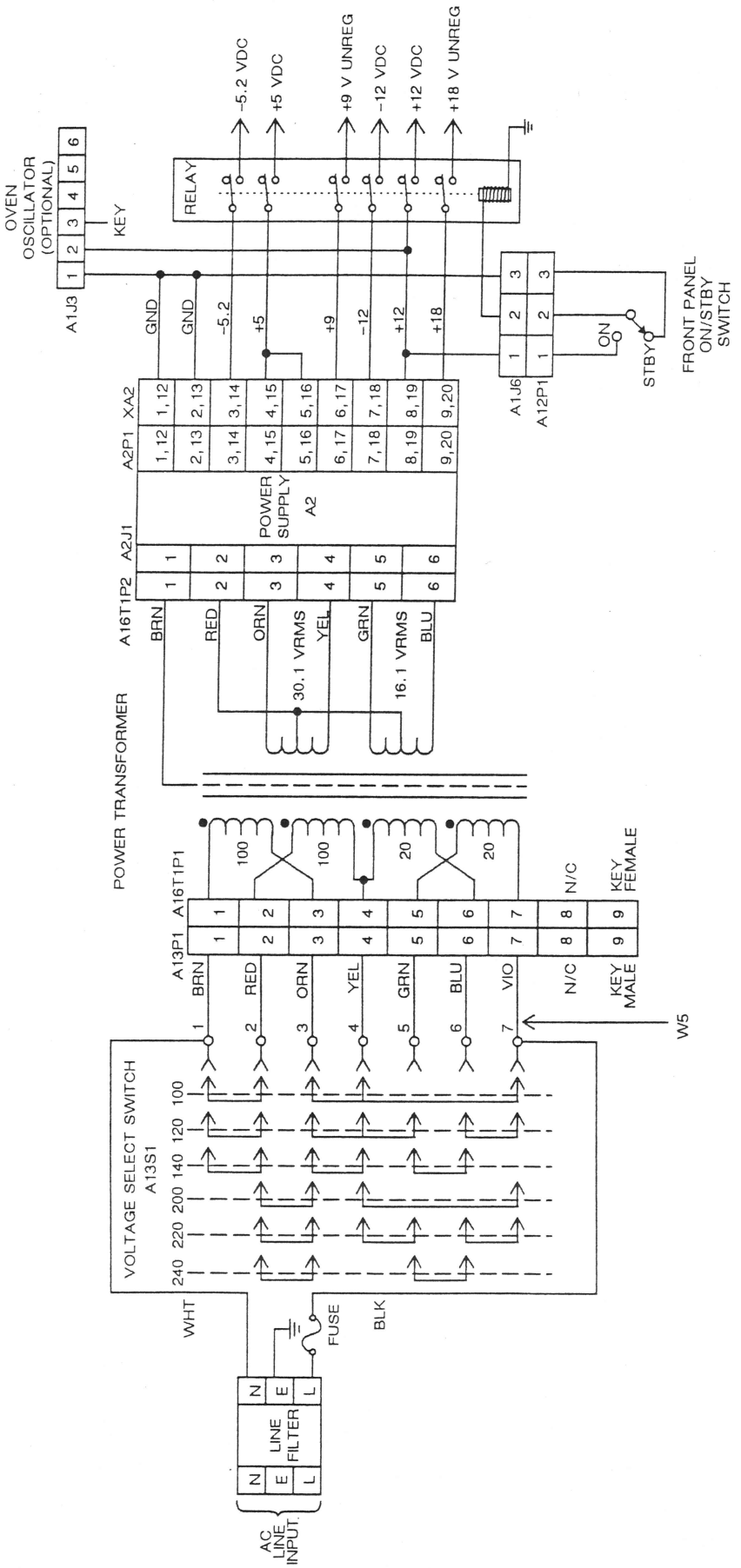



**Figure 10–5. Power Entry Schematic Diagram.**

## A1
## MOTHERBOARD
## 2020418-04

The primary purpose of the Motherboard assembly is to provide an electrical interface between the various sub-assemblies used in the counter. The Motherboard also contains a +5 volt regulator, a relay, and the circuitry used to control the speed of the fan.

The voltage regulator circuit, consisting of U1, C6 and C7, provides a separate +5 volt supply used to power the front panel display. The front panel display uses a separate dc supply to prevent digital noise, generated by the display, from interfering with the sensitive circuits used in the counter.

The relay is used to disconnect all dc voltages from the counter in the standby mode while still providing dc to the optional oven oscillator.

A fan control circuit varies fan speed as a function of the internal counter temperature. A thermistor is used to sense the internal temperature of the counter. As the temperature increases, the resistance of the thermistor decreases causing the voltage on the base of Q2 to increase. The increased voltage on the base of Q2 causes it to conduct harder which in turn causes Q1 to conduct harder, increasing fan speed and internal airflow. The value of resistor R4 determines the minimum fan speed.

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## A1 MOTHERBOARD 2020418-04 Rev. A

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,ELCTLT | 220µF | 20% | 35V | 2200033-00 | 2 |
| C2 | | CAP,DISC,CER | .1µF | | 50V | 2150092-00 | 1 |
| C3 | | CAP,TANTALUM | 47µF | 20% | 16V | 2300025-00 | 1 |
| C4 | | CAP,CER | .001µF | 20% | 100V | 2150001-00 | 2 |
| C5 | C1 | | | | | | |
| C6 | | CAP,TANTALUM | 10µF | 20% | 25V | 2300029-00 | 2 |
| C7 | C6 | | | | | | |
| C8 | C4 | | | | | | |
| C9 | | CAP,ML CER | 1µF | 20% | 50V | 2150023-00 | 1 |
| J1 | | CONN,PCB HEADER,26 PIN,W/EJCTR | | | | 2620078-00 | 2 |
| J2 | J1 | | | | | | |
| J3 | | CONN,FRICT LK 156,6 PIN | | | | 2620090-00 | 1 |
| J4 | | NOT USED | | | | | |
| J5 | | CONN,FRICT LK,HEADER,.156 13 PIN | | | | 2620151-00 | 1 |
| J6 | | CONN,PC,RCPT LK 156,3 PIN | | | | 2620201-00 | 2 |
| J7 | J6 | | | | | | |
| K1 | | RELAY,PWR,6PDT,12V | | | | 3900007-00 | 1 |
| L1 | | INDUCTOR,1.0µH | | | | 3510003-00 | 1 |
| Q1 | | XSTR,MJE520,NPN,PWR | | | | 4710003-00 | 1 |
| Q2 | | XSTR,2N4401,NPN,SW AND AMP | | | | 4704401-00 | 1 |
| R1 | | RES,CC | 5.1 | 1/4W | 5% | 4010519-00 | 1 |
| R2 | | RES,CC | 1.1K | 1/4W | 5% | 4010112-00 | 1 |
| R3 | | THERMISTOR CHIP | | | | 4340005-00 | 1 |
| R4 | | RES,CC | 240 | 1W | 5% | 4030240-00 | 1 |
| R5 | | RES,M/OX | 2.74K | 1/10W | 1% | 4052741-00 | 1 |
| R7 | | RES,M/OX | 1.50K | 1/8W | 1% | 4061501-00 | 1 |
| U1 | | IC,7805C,VOLT RGLTR,+5V,TO-220 | | | | 3057805-02 | 1 |
| XA2 | | CONN,PCB EDGE,AMPL,11 PIN | | | | 2620183-00 | 1 |
| XA5 | | CONN,PCB EDGE,2 X 30 PIN,.125 X.250 | | | | 2610150-00 | 3 |
| XA6 | XA5 | | | | | | |
| XA7 | | NOT USED | | | | | |
| XA8 | | NOT USED | | | | | |
| XA9 | XA5 | | | | | | |

HARDWARE USED IN THIS ASSEMBLY

| | | |
|---|---|---|
| SCR,PNH,X-REC,SEMS,INTL,4-40X3/8 | 5171004-06 | 2 |
| NUT,HEX,CRES 4-40 UNC-2B | 5180004-40 | 2 |
| HEATSINK,VERT PCB MT,TO-220 | 5000363-00 | 1 |
| SCR,PNH,X-REC,SEMS,INTL,4-40X1/4 | 5171004-04 | 1 |
| WASH,LK,INTL-T,CRES # 4 | 5163004-00 | 2 |
| PAD,INSULATOR,SILICON TO-126 | 5000236-00 | 1 |
| PCB SCHEMATIC DIAGRAM | 5500418-03 B | REF. |

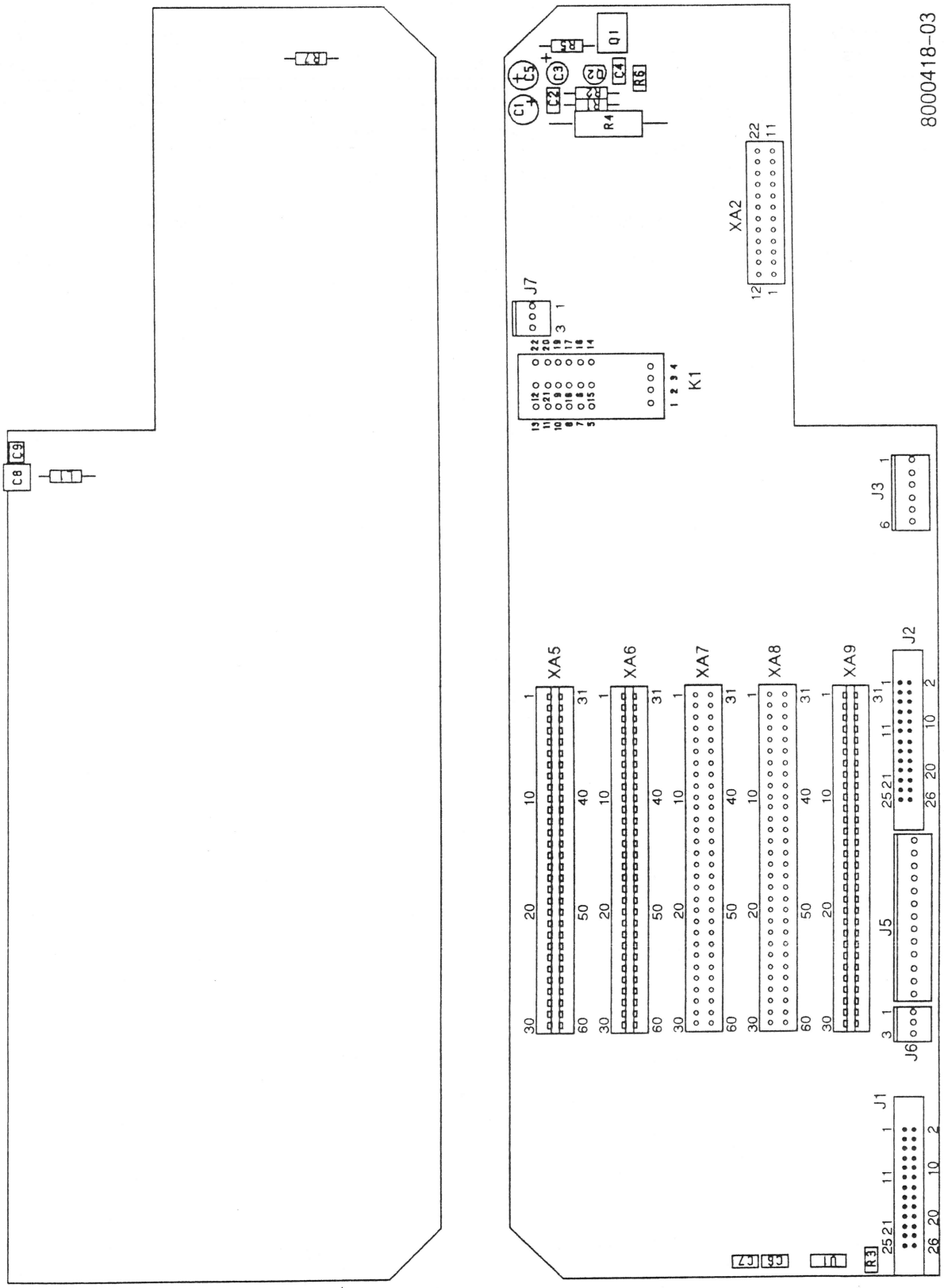
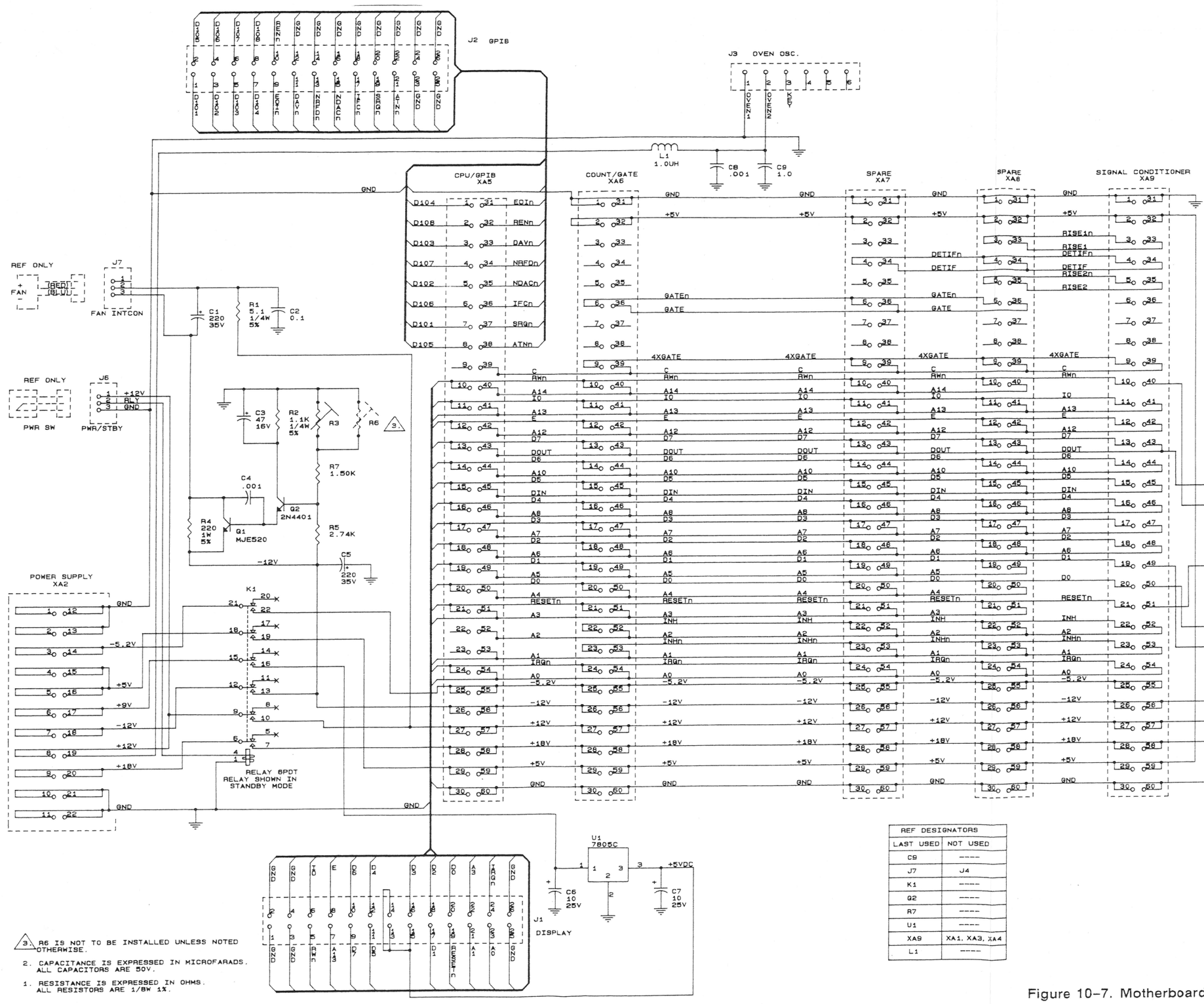



Figure 10-6. Motherboard (A1) Component Locator.




3. R6 IS NOT TO BE INSTALLED UNLESS NOTED OTHERWISE.

2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W 1%.

NOTES: UNLESS OTHERWISE SPECIFIED.

| REF DESIGNATORS | |
|---|---|
| LAST USED | NOT USED |
| C9 | ----- |
| J7 | J4 |
| K1 | ----- |
| Q2 | ----- |
| R7 | ----- |
| U1 | ----- |
| XA9 | XA1, XA3, XA4 |
| L1 | ----- |

5500418-03

Figure 10-7. Motherboard (A1) Schematic Diagra

## A2
## POWER SUPPLY
## (2020417-04)

The Power Supply assembly receives ac voltages of 16 Vrms and 30 Vrms from the secondary windings on the power transformer. These ac voltages are full wave rectified by CR1 and CR2 and provide two unregulated dc voltages: +9 and +18 V, and four regulated dc voltages: +5 V, -5.2 V, +12 V, and -12 V.

The positive rectified voltage from CR1 is filtered by C4 and used as the source for the +18 V unregulated supply. The +18 V unregulated supply is also fed to U2, a 12 V three terminal regulator. Variable resistor R3 provides adjustment for the +12 V supply.

The negative rectified voltage from CR1 is filtered by C5 and fed to U3, a -12 V three terminal regulator. Variable resistor R6 provides adjustment for the -12 V supply.

The positive rectified voltage from CR2 is filtered by C1 and used as the source for the +9 V unregulated supply. The +9 V unregulated supply is used to drive the front panel display. The +9 V unregulated supply is also fed to U1, a +5 V three terminal regulator. Jumpers W1 and W2 are provided for adjustment of the +5 V supply.

The negative rectified voltage from CR2 is filtered by C2 and fed to U4, a -5.2 V three terminal regulator. There is no adjustment provided for the -5.2 V supply.

Connector J3 provides an input for an external 12 V supply. This external supply connects to a rear panel connector and is used to power the optional oven oscillator during transit.

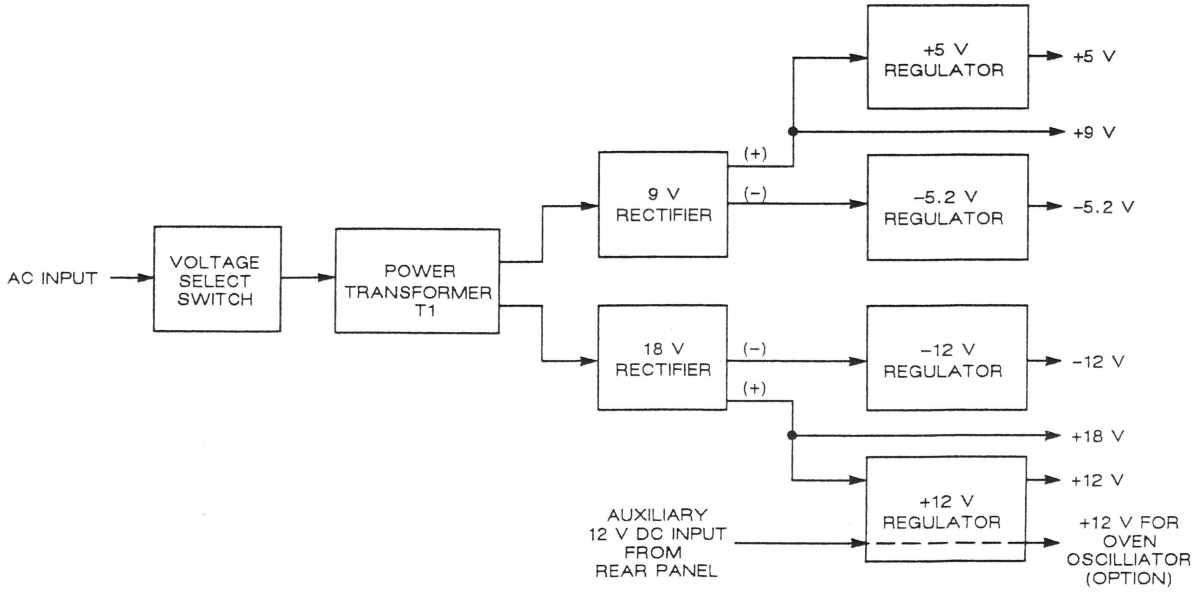



Figure 10-8. Power Supply Functional Block Diagram.

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## A2 POWER SUPPLY 2020417-04 Rev. B

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,ALUM ELCTLT | 33,000µF | | 16VDC | 2100130-00 | 2 |
| C2 | C1 | | | | | | |
| C3 | | CAP,TANTALUM | 10µF | 20% | 25V | 2300029-00 | 4 |
| C4 | | CAP,ALUM ELCTLT | 15,000µF | | 25VDC | 2100129-00 | 1 |
| C5 | | CAP,ALUM ELCTLT | 10,000µF | | 25VDC | 2100131-00 | 1 |
| C6 | C3 | | | | | | |
| C7 | | CAP,TANTALUM | 1µF | 20% | 35V | 2300008-00 | 3 |
| C8 | C3 | | | | | | |
| C9 | | NOT USED | | | | | |
| C10 | C3 | | | | | | |
| C11 | C7 | | | | | | |
| C12 | C7 | | | | | | |
| C13 | | CAP,ML CER | 1µF | 20% | 50V | 2150023-00 | 4 |
| C14 | C13 | | | | | | |
| C15 | C13 | | | | | | |
| C16 | C13 | | | | | | |
| C17 | | CAP,DISC,CER | .002µF | 20% | 1KV | 2150005-00 | 1 |
| CR1 | | DIODE,MDA970-2,BRIDGE,100V | | | | 2710045-00 | 1 |
| CR2 | | DIODE,MDA990-1,BRIDGE | | | | 2710028-00 | 1 |
| CR3 | | DIODE,1N4003,GP RECTIFIER | | | | 2700004-00 | 2 |
| CR4 | CR3 | | | | | | |
| CR5 | | DIODE,ZENER OVERVOLTAGE,SA16,16V | | | | 2700007-00 | 1 |
| J1 | | CONN,SQ POST,6 PIN,156 | | | | 2620157-00 | 1 |
| J2 | | CONN,SQ,POST,3 PIN,156 | | | | 2620154-00 | 1 |
| J3 | | CONN,POST,SQ 156,2 PIN | | | | 2620153-00 | 1 |
| L1 | | INDUCTOR,39µH,HIGH CURRENT | | | | 3510030-00 | 1 |
| R1 | | RES,M/OX | 475 | 1/10W | 1% | 4054750-00 | 1 |
| R2 | | RES,M/OX | 3.01K | 1/8W | 1% | 4053011-00 | 1 |
| R3 | | POT,CERMET,TO5 | 2K . | 5W | 10% | 4250016-00 | 2 |
| R4 | | NOT USED | | | | | |
| R5 | | NOT USED | | | | | |
| R6 | R3 | | | | | | |
| R7 | | RES,M/OX | 8.66K | 1/8W | 1% | 4068661-00 | 1 |
| R8 | | RES,M/OX | 1.21K | 1/10W | 1% | 4051211-00 | 1 |
| R9 | | RES,M/OX | 200 | 1/4W | 2% | 4130201-00 | 1 |
| R10 | | RES,CC | 5.6 | 1/4W | 5% | 4010569-00 | 1 |
| R11 | | RES,M/OX | 13 | 1/4W | 2% | 4130130-00 | 1 |
| R12 | | RES,CC | 4.7 | 1/4W | 5% | 4010479-00 | 1 |
| TP1 | | CONN,PIN-TP,SWAGE .040D-.150L | | | | 2620193-00 | 4 |
| TP2 | TP1 | | | | | | |
| TP3 | TP1 | | | | | | |
| TP4 | TP1 | | | | | | |
| U1 | | IC,78H05A,VOLT RGLTR,+5V,TO-3 | | | | 3057805-01 | 1 |
| U2 | | IC,LM350T,3A,RGLTR,ADJ,POS,TO-220 | | | | 3040350-00 | 1 |
| U3 | | IC,LM337,VOLT RGLTR,ADJ,NEG,TO-220 | | | | 3040337-00 | 1 |
| U4 | | IC,LM345-5.2,VOLT RGLTR,NEG,TO-3 | | | | 3040345-00 | 1 |

## A2 POWER SUPPLY (Continued) 2020417-04 Rev. B

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| HARDWARE USED IN THIS ASSEMBLY | | | | |
| | | BRACKET,HEATSINK,P.S. | 5210860-02 | 1 |
| | | PAD,INSULATOR,SILICON TO-220 | 5000235-00 | 2 |
| | | INSULATOR,SILICON TO-3 | 5000239-00 | 2 |
| | | NUT,HEX,CRES 4-40 UNC-2B | 5180004-40 | 4 |
| | | BUSHING,NYLON INSUL | 5000159-00 | 2 |
| | | SCR,PNH X-REC 6-32X3/4 UNC | 5120006-12 | 1 |
| | | SCR,PNH X-REC 4-40X3/16 UNC | 5120004-03 | 2 |
| | | WASH,LK,INTL-T,CRES # 4 | 5163004-00 | 8 |
| | | WASHER,FLAT,CRES,REDUCED O.D. NO.4 | 5161004-00 | 2 |
| | | SCR,PNH X-REC 6-32X1/4 UNC | 5120006-04 | 2 |
| | | WASH,LK,INTL-T,CRES # 6 | 5163006-00 | 3 |
| | | WIRE,BUS,18AWG | 5460011-00 | 10 |
| | | TUBING,TEFLON 18 AWG CLR | 5480012-00 | 9 |
| | | SCR,PNH X-REC 4-40X3/8 UNC | 5120004-06 | 4 |
| | | PCB SCHEMATIC DIAGRAM | 5500417-03 B | REF. |

Power Supply Component Locator
(PCB Assembly A2)

(See following page)

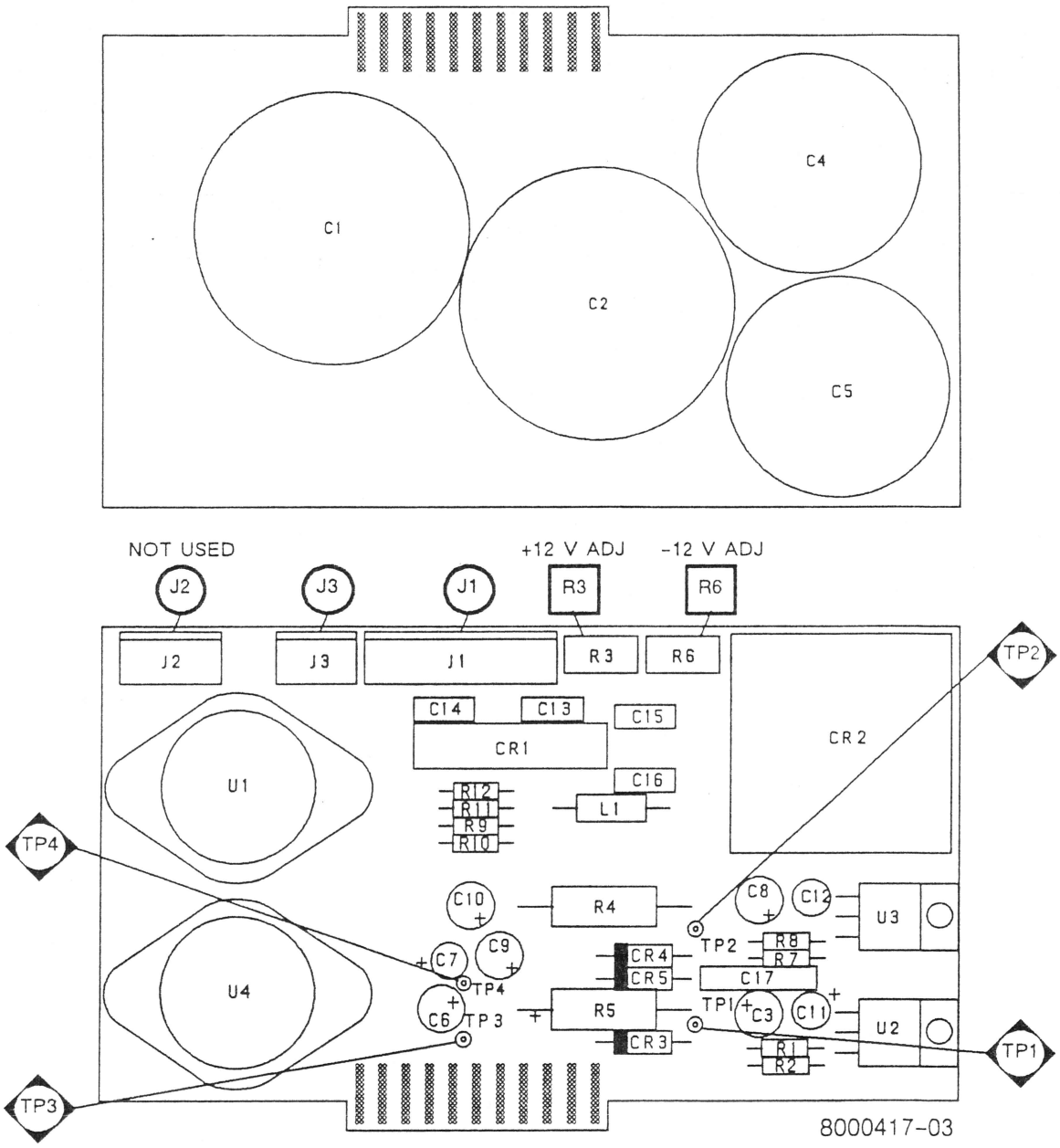
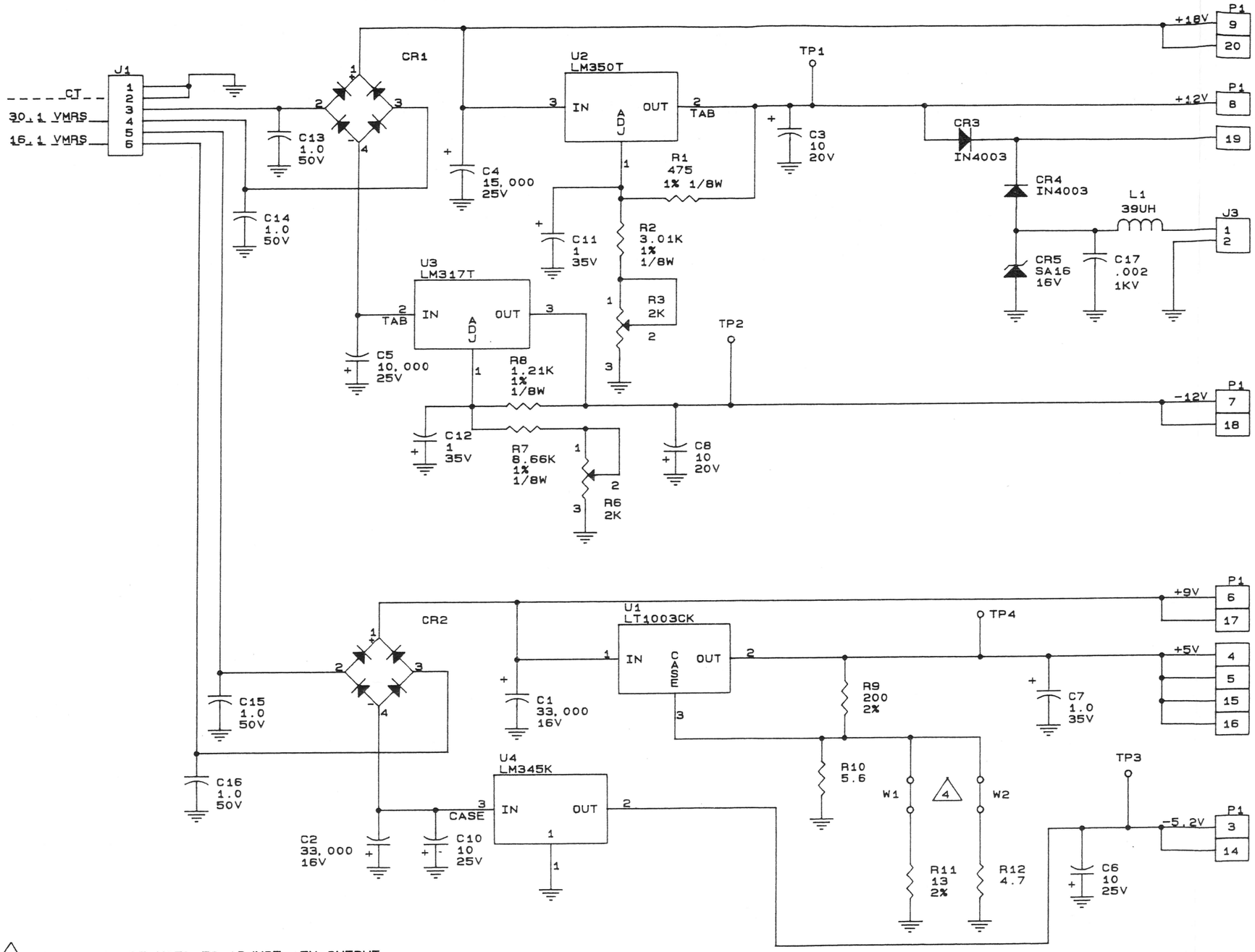



Figure 10-9. Power Supply (A2) Component Locator.




| LAST USED | NOT USED |
|---|---|
| C17 | C9 |
| J3 | J2 |
| R12 | R4, R5 |
| TP4 | ---- |
| U4 | ---- |
| W2 | ---- |
| CR5 | --- |
| L1 | --- |
| P1 | ---- |

4. W1 AND W2 ARE USED TO ADJUST +5V OUTPUT. SEE TEST PROCEDURE FOR DETAILS.

3. PREFIX FOR ALL REF. DESIG: A2.

2. ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.

1. ALL FIXED RESISTORS ARE 1/4W +/-5%. ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

5500417-0

Figure 10-10. Power Supply (A2) Schematic Diagra

## A5
## PROCESSOR/GPIB
## (2020416-01)

The Processor/GPIB assembly contains the microprocessor, control logic, and firmware used to control counter operations along with the GPIB Interface circuitry. The processor portion of this assembly can be divided into six functional blocks:

- Microprocessor
- Power-up reset circuit
- Address decoder
- Counter memory
- Control logic and buffers
- Serial-parallel converter

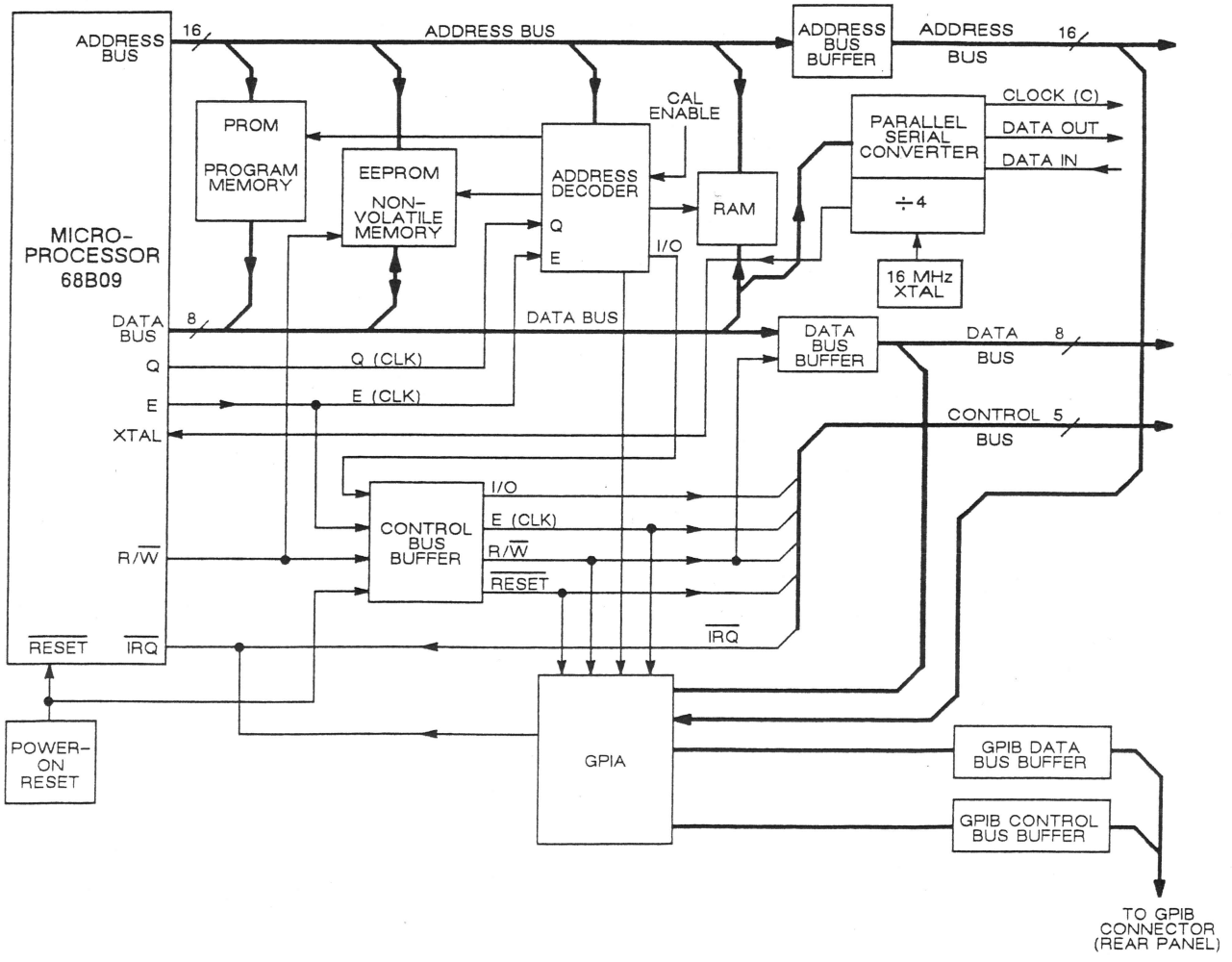



Figure 10-11. Processor/GPIB Functional Block Diagram.

## MICROPROCESSOR

The counter uses a Motorola 68B09 microprocessor (U12), which also contains the clock generation circuitry for the digital system. The NMI, FIRQ, and DMA functions of the 68B09 are not used, and their corresponding control lines are *always* disabled. The processor state indicators (BS and BA) also are not used. The $\overline{IRQ}$, $\overline{HALT}$, and MRDY control signals are connected through the edge connector to the Motherboard assembly (A1).

## POWER-UP RESET CIRCUIT

The power-up reset circuit, consisting of voltage comparator U13 and the associated circuitry, provides an active low reset signal for approximately 100 ms after the counter is first turned on. At turn-on, the voltage on U13 pin 3 is set to approximately 3.9 V by zener diode CR1, and the voltage on pin 2 is low, which causes the output from U13 to be low. C17 slowly charges through R6 until the voltage on U13 pin 2 exceeds the voltage on pin 3. This causes the output from U13 to go from low to high, removing the reset condition. R4 provides hysteresis. When power is removed, C17 quickly discharges through CR2.

## ADDRESS DECODER

Address decoding of the 64K byte address space is performed by programmable array logic (PAL) U5. The outputs from U5 enable the various memory devices depending on the input addresses of A9 through A15 and the status of the read/write (R/$\overline{W}$) line. U5 pin 15, CAL EN, is normally high to protect the portion of the EEPROM used for calibration tables. When performing calibration (Special Functions 91 and 92), this pin is grounded to allow information to be written to the calibration tables.

## COUNTER MEMORY

The processor contains three types of memory: programmed read only memory (PROM), nonvolatile RAM (EEPROM), and RAM.

### PROM MEMORY

The PROM memory contains the system program for the instrument, also known as instrument firmware. This program is contained in the upper 48K of a single 64K x 8 bit PROM (U9). Listed on the PROM is an EIP part number and a revision code that corresponds to the firmware contained in the particular instrument.

### NONVOLATILE RAM

The 8K x 8 bit nonvolatile RAM (U2) contains temporary information that must be retained even if the unit is powered down. This type of information includes: stored instrument setups, calibration tables, GPIB address, and unit configuration. The portion of this RAM that contains the calibration tables is normally protected to prevent the calibration information from being accidentally altered. During calibration a jumper is connected between U5 pin 15 and ground to allow information to be written to the protected portion of the memory.

### RAM

The 8K x 8 bit volatile RAM (U6) is used as temporary memory during operation of the counter. The microprocessor uses this memory to store all temporary variables used in the operation of the instrument.

The following is the memory map of the instrument:

| | |
|---|---|
| Volatile RAM Memory | 0000 - 0FFF |
| Nonvolatile RAM Memory | 3000 - 3FFF |
| I/O | 1000 - 2FFF |
| Program Memory | 4000 - FFEF |
| Reserved (68B09) | FFF0 - FFF1 |
| SW13 | FFF2 - FFF3 |
| SW12 | FFF4 - FFF5 |
| FIRQ | FFF6 - FFF7 |
| IRQ | FFF8 - FFF9 |
| SWI | FFFA - FFFB |
| NMI | FFFC - FFFD |
| RESET | FFFE - FFFF |

## CONTROL LOGIC AND BUFFERS

The counter digital system contains three buses: the data bus, the address bus, and the control bus.

### DATA BUS

The data bus originates in the microprocessor and is connected to the rest of the instrument via the Motherboard. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing program header E1. The data bus on the Processor/GPIB assembly is buffered from the rest of the digital system and is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/$\overline{W}$ control line.

### ADDRESS BUS

The address bus also originates in the microprocessor and is connected to the rest of the instrument via the main interconnect board. The address bus buffers (U7 and U10) are always enabled.

### CONTROL BUS

The control bus contains eight control lines, five of which originate on this assembly. The other three control lines originate in the rest of the digital system.

R/$\overline{W}$, E, and Q originate in the microprocessor. $\overline{\text{RESET}}$ is supplied by the power-up reset circuit. The I/O control line is true when A15 and A14 from U12 are at logic 0 and either A13, A12, or both are at logic 1 levels. The $\overline{\text{IRQ}}$ control line is the wired-OR of all the interrupt request lines. MRDY is the wired-OR of all the memory ready control lines. The MRDY and $\overline{\text{HALT}}$ control lines are provided for future expansion

## SERIAL-PARALLEL CONVERTER

The serial-parallel converter performs the following functions:

- Provides a 4 MHz clock for the microprocessor by dividing the 16 MHz crystal oscillator clock (Y1) by four. The divided 4 MHz signal is applied to the microprocessor at pin 38, which connects the signal to the on-chip oscillator for use in timing control.
- Converts the parallel information from the data bus to serial. The serial output has two associated lines: C (U14 pin 20) and DOUT (U14 pin 4).
- Converts the serial data information at DIN (U14 pin 14) to parallel for output at pins D0 through D7.

## GPIB INTERFACE

The GPIB interface makes the 625A counter fully compatible with IEEE 488 - 1978. The functions implemented are:

- Basic talker with talk only
- Basic listener
- Remote/local with local lockout
- Device clear
- Device trigger
- Service request

The general purpose interface adapter (GPIA) (U1) performs all the GPIB functions and protocols according to commands from the microprocessor. All data and messages between the microprocessor and the GPIB are transferred through U1.

Transceivers U3 and U4 provide the required bus buffering and termination for the GPIB. They are driven directly from the GPIA.

Refer to Section 4 for programming information on the GPIB interface.

## A5 PROCESSOR/GPIB 2020416-01 Rev. C

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,ML CER | .01µF | 10% | 100V | 2150014-00 | 15 |
| C2 | C1 | | | | | | |
| C3 | C1 | | | | | | |
| C4 | C1 | | | | | | |
| C5 | C1 | | | | | | |
| C6 | C1 | | | | | | |
| C7 | C1 | | | | | | |
| C8 | C1 | | | | | | |
| C9 | C1 | | | | | | |
| C10 | C1 | | | | | | |
| C11 | | CAP,TANTALUM | 33µF | 20% | 10V | 2300015-00 | 1 |
| C12 | C1 | | | | | | |
| C13 | C1 | | | | | | |
| C14 | | NOT USED | | | | | |
| C15 | | NOT USED | | | | | |
| C16 | C1 | | | | | | |
| C17 | | CAP,TANTALUM | 3.9µF | 10% | 15V | 2300027-00 | 1 |
| C18 | C1 | | | | | | |
| C19 | C1 | | | | | | |
| CR1 | | DIODE,1N5228,ZENER 3.9V | | | | 2705228-00 | 1 |
| CR2 | | DIODE,5082-2835,PSVT SCHOTTKY | | | | 2710004-00 | 1 |
| E1 | | HEADER,PROGRAM DIP 16 PIN | | | | 5000205-00 | 1 |
| R1 | | RES,M/OX | 4.75K | 1/8W | 1% | 4064751-00 | 5 |
| R2 | R1 | | | | | | |
| R3 | R1 | | | | | | |
| R4 | | RES,M/OX | 301K | 1/8W | 1% | 4063013-00 | 1 |
| R5 | | RES,M/OX | 243 | 1/8W | 1% | 4062430-00 | 1 |
| R6 | | RES,M/OX | 22.1K | 1/8W | 1% | 4062212-00 | 1 |
| R7 | | RES,M/OX | 1M | 1/8W | 1% | 4061004-00 | 1 |
| R8 | | RES,M/OX | 30.1K | 1/8W | 1% | 4063012-00 | 1 |
| R9 | R1 | | | | | | |
| R10 | R1 | | | | | | |
| RN1 | | RES,NTWK | 9X10K | 0.2W | 2% | 4170003-00 | 3 |
| RN2 | RN1 | | | | | | |
| RN3 | RN1 | | | | | | |
| TP1 | | CONN,PCB,.040D PIN,GOLD | | | | 2620032-00 | 7 |
| TP2 | TP1 | | | | | | |
| TP3 | TP1 | | | | | | |
| TP4 | TP1 | | | | | | |
| TP5 | TP1 | | | | | | |
| TP6 | TP1 | | | | | | |
| TP7 | TP1 | | | | | | |
| U1 | | IC,TMS9914A,GPIB CONTROLLER | | | | 3059914-00 | 1 |
| U2 | | IC,X2864B,8KX8,EEPROM | | | | 6500042-01 | 1 |
| U3 | | IC,75160A,GP INTERFACE BUS XCVR | | | | 3055160-00 | 1 |
| U4 | | IC,75161 | | | | 3050161-00 | 1 |
| U5 | | PAL,PROGRAMMED,ADDRESS DECODER | | | | 2070085-02 | 1 |
| U6 | | IC,HM6264P,8192X8BIT CMOS RAM | | | | 3000014-00 | 1 |
| U7 | | IC,74LS244 | | | | 3084244-00 | 2 |
| U8 | | IC,74LS245 | | | | 3084245-00 | 1 |
| U9 | | NOT USED | | | | | |

## A5 PROCESSOR/GPIB (Continued) 2020416-01 Rev. C

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| U10 | U7 | | | |
| U11 | | IC,74LS365 | 3084365-00 | 1 |
| U12 | | IC,68B09,MP,8-BIT,2 MHZ | 3050025-00 | 1 |
| U13 | | IC,LM311,VOLT COMPARATOR | 3050311-00 | 1 |
| U14 | | PLD,PRGM,FREQ DIV,SER/PAR,5032PC | 2750001-01 | 1 |
| U15 | | OSC,CRYSTAL CLOCK,16MHZ .05% | 2030060-00 | 1 |
| XE1 | | CONN,SOCKET,DIP,16 PIN | 2630016-00 | 1 |
| XU1 | | NOT USED | | |
| XU2 | | NOT USED | | |
| XU3 | | NOT USED | | |
| XU4 | | NOT USED | | |
| XU5 | | NOT USED | | |
| XU6 | | NOT USED | | |
| XU7 | | NOT USED | | |
| XU8 | | NOT USED | | |
| XU9 | | CONN,SOCKET,DIP,28 PIN | 2630021-00 | 1 |
| XU10 | | NOT USED | | |
| XU11 | | NOT USED | | |
| XU12 | | NOT USED | | |
| XU13 | | NOT USED | | |
| XU14A | | CONN,SOCKET,DIP,14 PIN | 2630015-00 | 2 |
| XU14B | XU14A | | | |
| HARDWARE USED IN THIS ASSEMBLY | | | | |
| | | HANDLE,PCB | 5230001-00 | 2 |
| | | PIN,ROLL,3/32 DIA 1/4 LG | 5110008-00 | 2 |
| | | WIRE,INSUL,30AWG,GREEN | 5430555-00 | 3 |
| | | PCB SCHEMATIC DIAGRAM | 5500416-01 C | REF. |

Processor/GPIB Component Locator
(PCB Assembly A5)

(See following page)

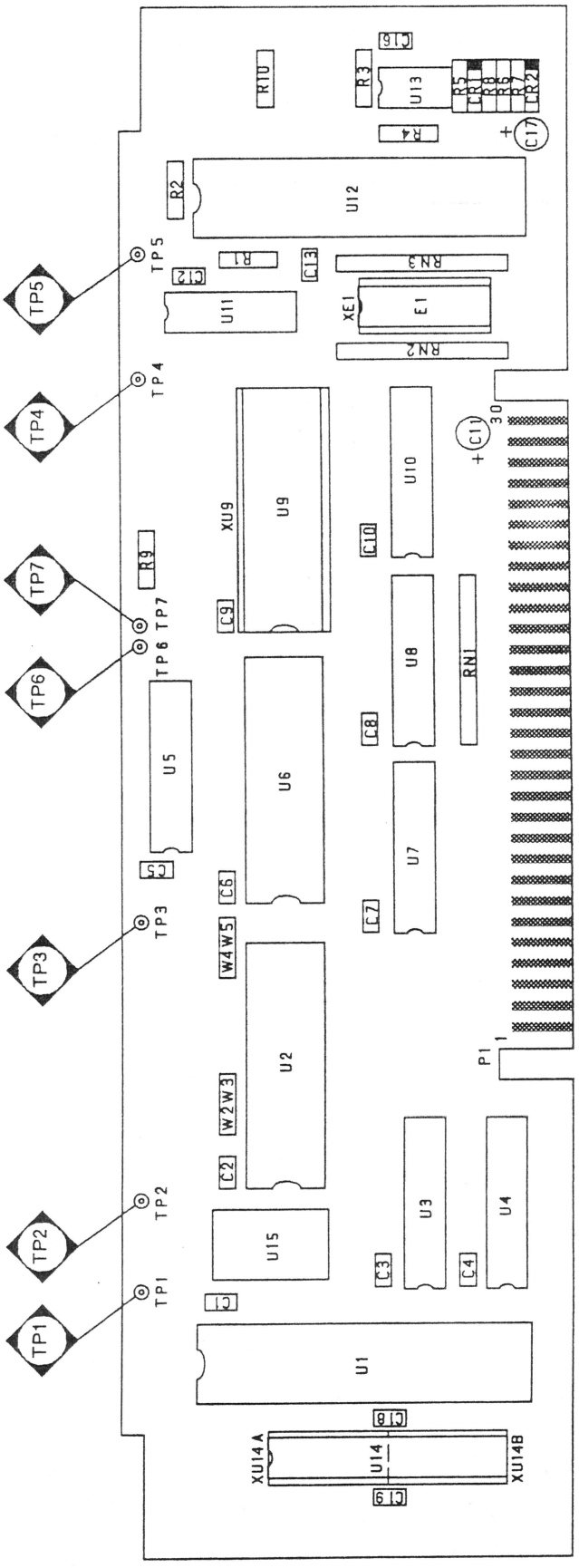
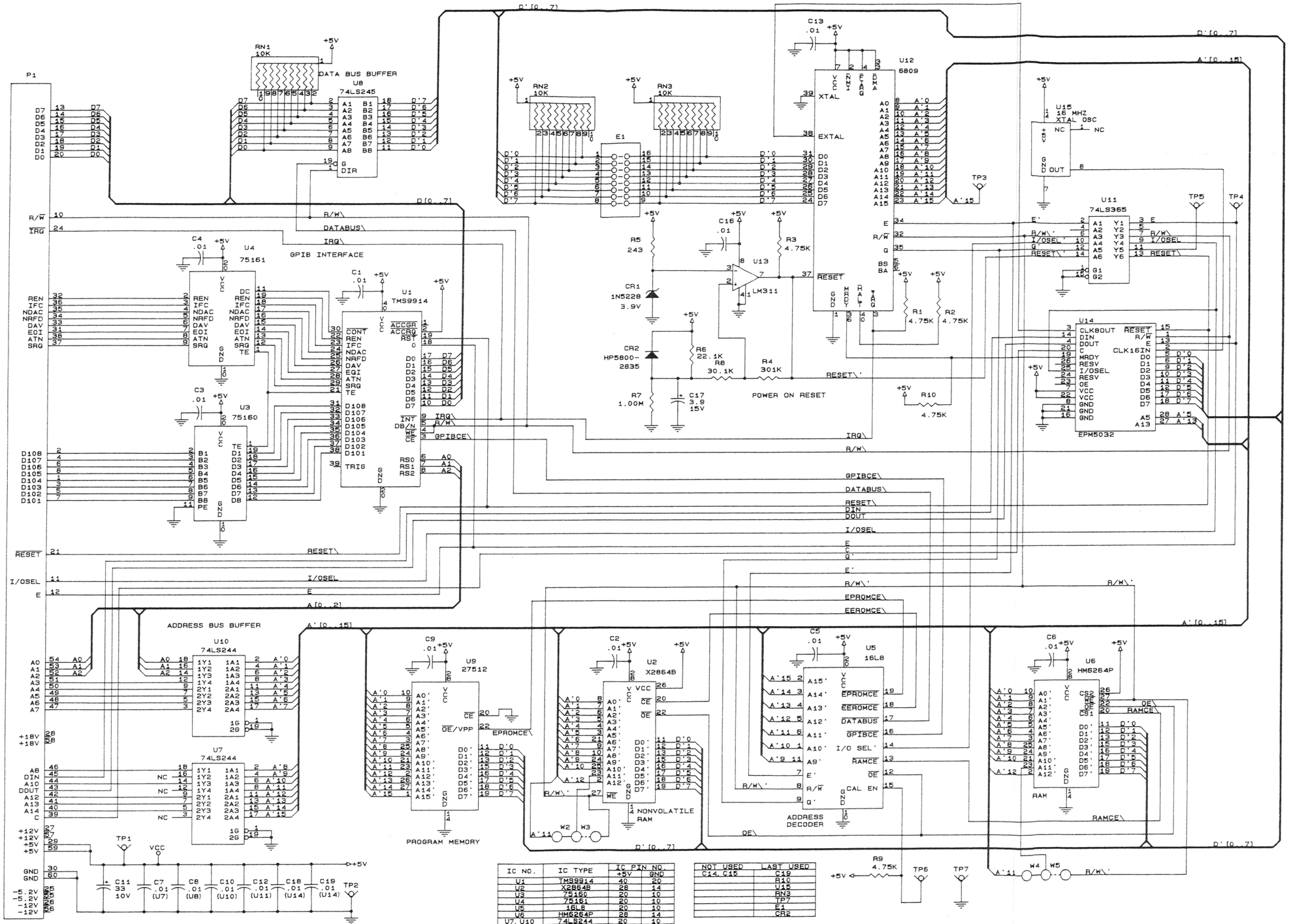



Figure 10-12. Processor/GPIB (A5) Component Locator.




| IC NO. | IC TYPE | IC PIN NO. +5V | IC PIN NO. GND |
|---|---|---|---|
| U1 | TMS9914 | 40 | 20 |
| U2 | X2864B | 28 | 14 |
| U3 | 75160 | 20 | 10 |
| U4 | 75161 | 20 | 10 |
| U5 | 16L8 | 20 | 10 |
| U6 | HM6264P | 28 | 14 |
| U7, U10 | 74LS244 | 20 | 10 |
| U8 | 74LS245 | 20 | 10 |
| U9 | 27512 | 28 | 14 |
| U11 | 74LS365 | 16 | 8 |
| U12 | 6809 | 7 | 1 |
| U13 | LM311 | 8 | 1, 4 |
| U14 | EPM5032 | 7, 22 | 8, 21 |

| NOT USED | LAST USED |
|---|---|
| C14, C15 | C19 |
| | R10 |
| | U15 |
| | RN3 |
| | TP7 |
| | E1 |
| | CR2 |

2. CAPACITANCE IS EXPRESSED MICROFARADS. ALL CAPACITORS ARE 50V.
1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W 1%.
NOTES: UNLESS OTHERWISE SPECIFIED

5500416-01 C

Figure 10-13. Processor/GPIB (A5
Schematic Diagram

# A6
# COUNT CHAIN/GATE
# (2020421-03)

The Count Chain/Gate assembly consists of two functionally distinct circuits. The first is the gate generation circuitry which provides the precise gate time interval required for frequency measurements. The second is the count chain circuitry which counts the number of zero-crossings of the input signal occurring during the gate time interval.

## GATE CIRCUITRY

The gate circuitry consists of the following functional blocks:

- 10 MHz time base
- Internal/external time base select
- Time base divider
- Clock select
- Gate generator

### GENERAL DESCRIPTION

The internal 10 MHz time base signal, or alternatively the external time base signal, is selected by the time base select circuitry and used to provide an accurate time reference. This signal is used for gate generation and as the frequency reference for the phase-locked VCO (used as the local oscillator for downconversion). While using the internal time base, a sample of this signal is applied to the 10 MHz IN/OUT connector on the rear panel of the counter. This allows for the use of the internal time base as a system reference.

The 10 MHz signal used for gate generation is applied to a synchronous divide-by-100 circuit, consisting of U4 and U5, where it is divided down to a 100 kHz signal. To compensate for prescaling the Band 2 input signal by a factor of four, the gate time must be increased by the same factor. This is accomplished by again dividing the clock, by a factor of four, down to 25 kHz. The divided clock is applied to the gate generator circuit which, through microprocessor control, provides a gate signal with the precise time interval required by the count chain for frequency measurements.

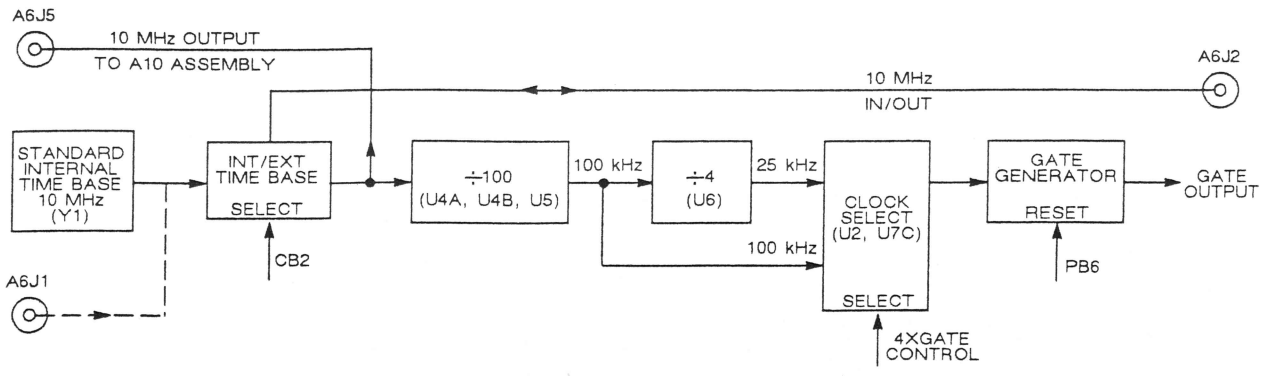



Figure 10-14. Gate Generation Functional Block Diagram.

## 10 MHz TIME BASE

The internal 10 MHz time base provides the time reference required for frequency measurements. The frequency accuracy of this signal determines how accurately the counter can perform frequency measurements. The standard time base used in the counter is a TCXO (Temperature Compensated Crystal Oscillator) which is physically mounted on this assembly, designated as Y1. An optional high stability ovenized time base is available for the counter which can improve the measurement accuracy of the instrument. On counters with this option, the standard TCXO is replaced by connector J1, which connects to the high stability time base.

## INTERNAL/EXTERNAL TIME BASE SELECT

The time base select circuitry allows the user to select between the internal time base and an external 10 MHz signal applied at the rear panel 10 MHz IN/OUT connector.

In the internal mode, the 10 MHz signal from the internal time base (Y1) is applied to buffer amplifier Q6. Q6 then amplifies the signal and provides the isolation necessary to maintain a constant load on the internal time base. In the internal mode, Q2 is turned off which allows Q5 to pass the signal from the emitter of Q6 to the base of Q7. Q7 serves as an emitter follower which drives the rear panel 10 MHz IN/OUT connector. The signal from the collector of Q6 is applied to pin 12 of U1D, a NAND gate which also serves as a Schmitt trigger, for sine wave to square wave conversion. When the internal time base is selected, the signal at U1A pin 2 is a TTL low causing the output from U1A pin 3 to be a TTL high. The TTL high from U1A pin 3 is applied to U1D pin 13 causing the 10 MHz signal on U1D pin 12 to be passed through to U1C pin 9. In the internal mode, the signal on U1C pin 10 is a TTL high causing the 10 MHz signal on U1C pin 9 to be passed through to U1C pin 8, the output of the time base select circuit.

In the external mode, a 10 MHz external time base signal from the rear panel 10 MHz IN/OUT connector is applied through C3 and R10 to the base of emitter-follower Q3. In the external mode Q1 is turned off which allows Q4 to pass the external 10 MHz signal from the emitter of Q3 to U1B pin 4, a NAND gate which also serves as a Schmitt trigger. Selecting the external time base mode causes the microprocessor to set U1B pin 5 (CB2) high causing the 10 MHz signal on U1B pin 4 to be passed through to U1C pin 10. In the external mode, the signal on U1C pin 9 is a TTL high. This causes the 10 MHz signal on U1C pin 10 to be passed through to U1C pin 8, the output of the time base select circuit.

The 10 MHz output from the time base select circuitry follows two paths. One path is through U2D, a 50 ohm inverting buffer/driver. The signal output at U2D pin 11 is fed to a low pass filter, consisting of L1, C9, and C12. This filter converts the signal back to a sine wave by reducing its harmonic content. The 10 MHz sine wave from J5 is routed to the microwave converter, where it serves as the frequency reference for the phase-locked VCO. The second path out of the time base select circuitry feeds the signal to the divider/gate generation circuitry.

## TIME BASE DIVIDER

The divider circuit receives the 10 MHz square wave reference from the time base select circuitry and synchronously divides it down into two clock signals: a 100 kHz signal and a 25 kHz signal. By synchronously dividing the input, transitions in both the 100 kHz and 25 kHz clock signals occur only during transitions of the 10 MHz reference signal. The 100 kHz signal is obtained by dividing the input signal by a factor of 100 in U4A, U4B, and U5. The 25 kHz signal is obtained by dividing the 100 kHz signal by a factor of 4 using U6, which consists of two D-type flip-flops.

## CLOCK SELECT CIRCUIT

Both the 100 kHz and the 25 kHz signals are fed to the clock select circuit consisting of NOR gate U7C and NAND gates U2A, U2B, and U2C. When Band 2 is selected the 4XGATE CTRL signal on U2B pin 5 will be high, causing the 25 kHz signal to pass through to U2C pin 9. The 4XGATE CTRL signal is also applied to U7C pins 8 and 9, which is being used as an inverter, causing the output at pin 10 to be low. The low from U7C pin 10 is applied to U2A pin 1 disabling the gate. This blocks the 100 kHz signal on U2A pin 2, and causes the output at U2A pin 3 to go high. The high from U2A pin 3 is applied to U2C pin 10, allowing the 25 kHz signal on U2C pin 9 to be passed through to U2C pin 8, the output of the clock select circuit.

Whenever Band 2 is not selected the 4XGATE CTRL signal on U2B pin 5 and U7C pins 8 and 9 is low, which blocks the 25 kHz signal at U2B pin 4 and causes the output from U2B pin 6 to be high. The low on U7C pins 8 and 9 causes the output on U7C pin 10 to be high. The high from U7C pin 10 is applied to U2A pin 1 causing the 100 kHz signal on pin 2 to be passed through to U2C pin 10. The other input to U2C pin 9, is high whenever Band 2 is not selected This causes the 100 kHz clock signal to be passed through to U2C pin 8, the output of the clock select circuit.

## GATE GENERATOR

The purpose of the gate generator is to provide an accurate stable time interval (GATE) required by the count chain for frequency measurements. This time interval referred to as gate time is switchable in decade increments between 100 microseconds and 1 second; or alternatively 400 microseconds to 4 seconds in Band 2. The gate generator consists of a programmable divide-by-N counter (U3), a dual flip-flop (U8A, U8B), an ECL flip-flop (U9A) and the associated logic gates (U7A,U7B,U7D). The divide ratio of U3, which determines the gate time, is set by U3 pins 12, 13, and 14 as follows:

**Table 10-2. Programmable Divide Ratio.**

| A6U3: | Pin 12 | Pin 13 | Pin 14 | Divide Ratio | Gate Time | Resolution |
|---|---|---|---|---|---|---|
| | 0 | 0 | 1 | 10 | 100 µs | 10 kHz |
| | 0 | 1 | 0 | 100 | 1 ms | 1 kHz |
| | 0 | 1 | 1 | 1000 | 10 ms | 100 Hz |
| | 1 | 0 | 0 | 10,000 | 100 ms | 10 Hz |
| | 1 | 0 | 1 | 100,000 | 1 s | 1 Hz |
| | 1 | 1 | 0 | 1,000,000 | 10 s | 0.1 Hz |

The gate generation timing diagram, Figure 10-14, is used as a reference for the following description of the gate generation sequence. The time designators in parentheses (T0...T3) correspond to points on the timing diagram.

The gate generation process begins (T0) by the microprocessor initializing the circuit by driving PB6 low, causing U8B pin 8 to go low. The low from U8B pin 8 clears U8A causing U8A pin 6 to go high, resetting programmable divider U3. After circuit initialization, the microprocessor begins gate generation by driving CA2 low (T1). This causes U8B pin 8 to go high, releasing control of flip-flop U8A. On the next low to high transition of the clock at U8A pin 3, flip-flop U8A toggles to the Q state (T2), removing the reset condition on U3 pin 4. At that point, U3 begins dividing down the input clock,

using the divide ratio selected by the data on U3 pins 12, 13, and 14. Halfway through the gate interval, U3 pin 1 will go high (T3). At the end of the gate interval U3 pin 1 makes a high to low transition, causing U8B pin 8 to go low and clearing U8A. This causes the output at U8A pin 6 to go high, returning the programmable divider to the reset state (T4). The output level at U8A pin 6 is monitored by the microprocessor, via PA7, to determine when the gate is complete.

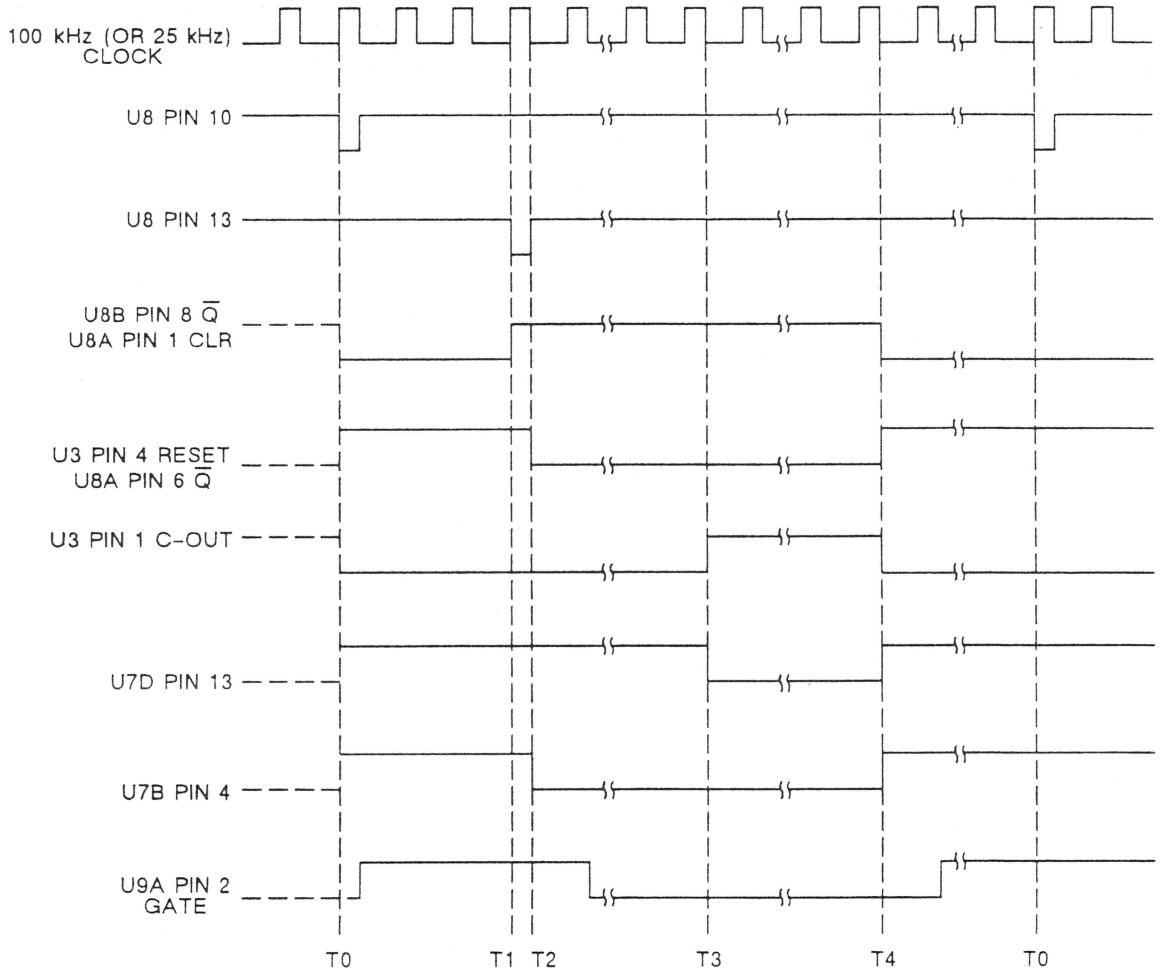



Figure 10-15. Gate Generator Timing Diagram.

The gate output at U8A pin 5 is inverted by U7B and applied to a TTL to ECL level translator consisting of R24, R25, and R26. The gate signal is applied to the data (D) input on U9A pin 7, an ECL flip-flop. The clock (100 kHz or 25 kHz) is used to clock the gate signal through to the Q output of U9A. This ensures that the gate begins and ends coincident with high to low transitions of the clock, thereby minimizing potential gate error.

Capacitor C6 is a select-at-test part (SAT), which provides some fine adjustment on the duration of the gate width to compensate for the input capacitance on U9A pin 6. The proper value is selected by placing the counter in the 100 MHz self-test mode, with 1 Hz resolution, and selecting a value of C6 that causes the counter to display exactly 100 MHz. Increasing the value of C6 slightly increases the gate width, causing the displayed count to increase.

## COUNT CHAIN

The count chain circuit consists of the following functional blocks:

- IF output buffer
- IF pulse-shaping network
- IF measurement circuit
- Real-time clock

### GENERAL DESCRIPTION

The count chain circuitry performs the actual frequency measurement for the counter. The IF signal, from the Signal Conditioner (A9), is applied at J3. The IF signal is an ECL signal with a frequency range of 10 Hz to 250 MHz. The IF signal divides at J3 and is routed to both the IF buffer and to the wave-shaping circuitry. The wave-shaping circuitry converts the IF signal into a series of narrow pulses prior to being applied to the 9-decade count chain. Frequency measurement is made by passing the IF to the count chain for a precise interval of time, known as the gate time. The count chain counts the number of zero crossings that occur while the gate is open and latches this information as BCD data. Upon completion of the gate, the latched data is read by the microprocessor, via PIA (U14), and the IF frequency is calculated by dividing the number of cycles measured by the gate time. Thus, if 100 cycles are counted within a gate time of 1 second, then the calculated IF frequency is 100 Hz.

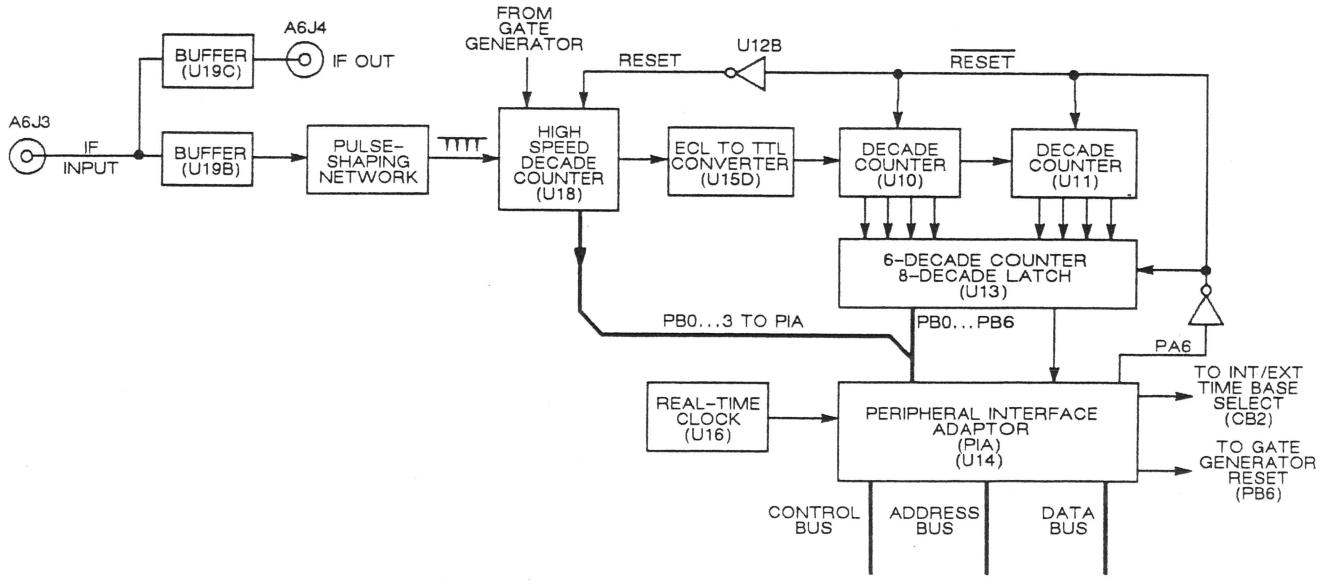



**Figure 10-16. Count Chain Circuit Functional Block Diagram.**

### IF OUTPUT BUFFER

The IF output buffer provides an ac coupled sample of the IF signal at J4. This sample is provided primarily as a troubleshooting aid, but can also be used for base band signal analysis. The circuit consists of an ECL line receiver, U19C, and the associated components. Since the output is ac coupled by capacitor C41, the output at J4 rolls off below 1 MHz.

### IF PULSE-SHAPING NETWORK

The IF signal from J3 is applied to differential line receiver U19B, which converts the single ended input into a differential output. The output of U19B at pins 6 and 7 is applied to a differential amplifier consisting of Q8 and Q9. Transistor Q13 acts as a diode, reducing the voltage on the collector of Q8 by approximately 0.7 volts with respect to the collector of Q9. The offset compensates for the emitter-base junction voltage of current switch Q11. This causes Q11 to switch between cutoff and saturation with relatively small changes of the input signal, effectively squaring up the output signal. The collector of Q11 drives an inductor (L2) which converts the current square wave into a series of positive pulses when Q11 turns on, and negative pulses when it turns off. These pulses are applied to pulse inverter Q12 which is a high-speed zero-crossing amplifier because it is biased at cutoff by Q14. Transistor Q14 performs as a diode. It is the same type of transistor as Q12, and is used for precise tracking over temperature. Amplifier Q12 inverts the positive pulses and removes the unwanted negative pulses.

### IF MEASUREMENT CIRCUIT

The IF measurement circuit consists of the following major parts:

- A high-speed ECL decade counter with BCD outputs (U18) and an associated bias circuit.
- Two 4-bit decade counters with BCD outputs (U10 and U11).
- A 6-decade counter with 8-decade latches and a multiplexed BCD output (U13).

The first decade counter, U18, is a high-speed ECL device; it receives negative-going ECL-level pulses at the clock input on pin 14. A bias tracking circuit, consisting of U17 and Q10, offsets the dc voltage at U18 pin 14 by 1 volt from the bias voltage at U18 pin 4. This offset causes U18 to trigger at approximately the 50% point on the input pulse, thereby increasing the noise immunity of the circuit.

While an active-low gate signal is applied to U18 pin 16, the counter is clocked by the input pulses at pin 14, and a divided-by-ten ECL output signal is available from U18 pin 9. This signal is converted from ECL to TTL by U15D and applied to U10, the second decade counter. The "D" output from U10 is applied through inverter U12A to the clock input of U11, the third decade counter. The last six decades of counting are performed by U13, a 6-decade counter/8-decade latch. The BCD output pins from both the second and third decade counters are connected to U13. The clock for U13 is derived internally from the C and D outputs of U11.

Upon completion of the gate, the BCD data is read by the microprocessor through PIA, U14. This process begins with the microprocessor sending an active-low, load data command to U13 pin 21. This causes U13 to latch the 8-decades of BCD data. The microprocessor then sends an active-high, scan reset command to U13 pin 1. This causes U13 to place the data for the most significant digit (MSD) on its BCD output, pins 17, 18, 19, and 20. The microprocessor reads the data, via the PIA, and then sends an active-low scan command to U13 pin 39. This causes U13 to place the data for the next most significant digit on its BCD output pins. This process continues until the microprocessor has read the first 8 digits of BCD data from U13. The microprocessor then reads the BCD data for the least significant digit from U18 pins 2, 7, 8, and 10. At the completion of the read cycle, the microprocessor sends a reset command (PA6) which resets the circuitry in preparation for the next count cycle.

### REAL-TIME CLOCK

The real-time clock, U16, supplies a 100 Hz signal to U14 pin 18. This signal is used by the microprocessor for the timing of software related functions such as the flashing of the annunciators on the front panel.

Setup Parameters: All at 100 MHz @ 0 dBm into Band 2.

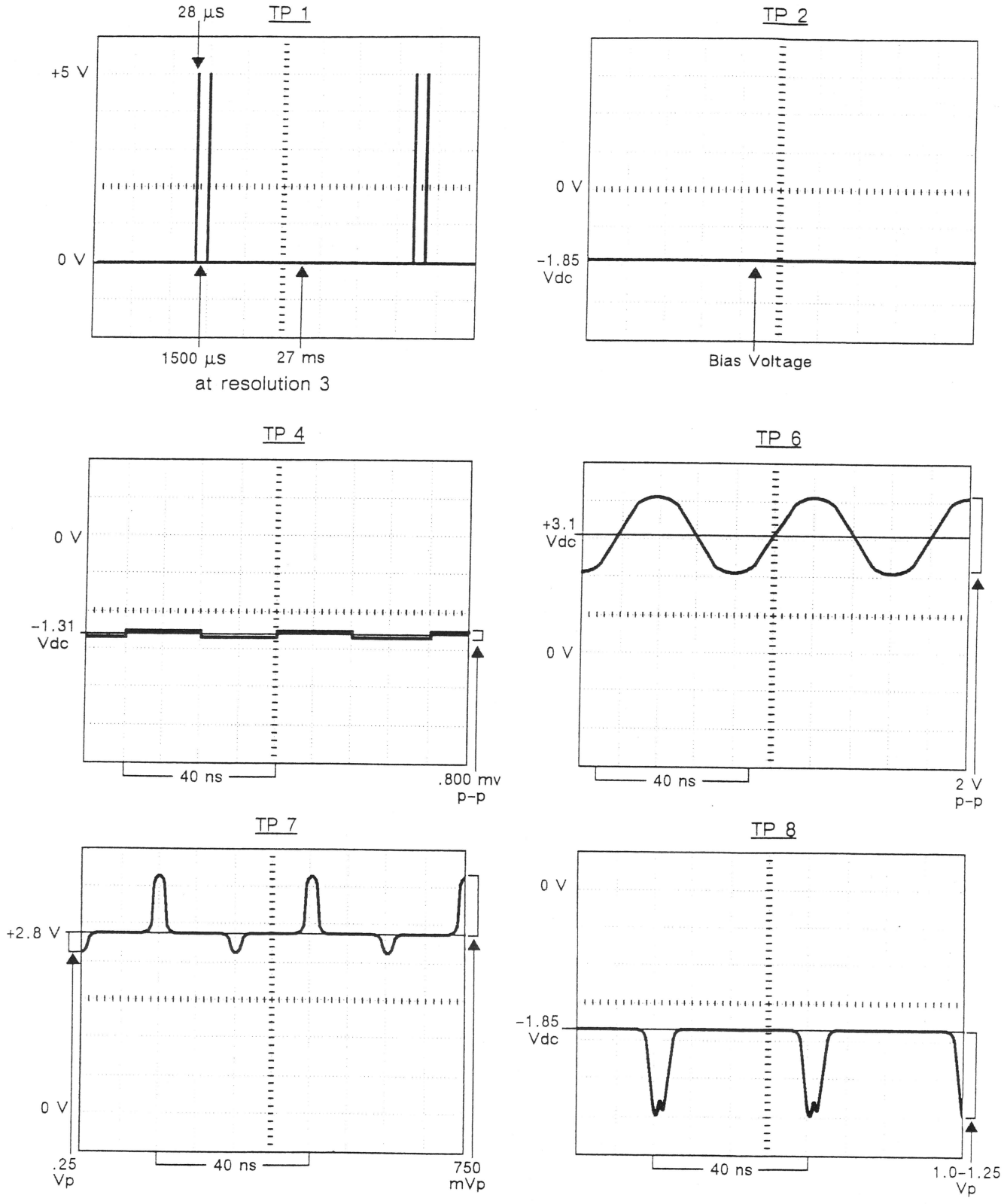



Figure 10-17. Count Chain/Gate Testpoint Waveforms.

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## A6 COUNT CHAIN/GATE 2020421-03 Rev. B

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,ML CER | .01µF | 10% | 100V | 2150014-00 | 37 |
| C2 | C1 | | | | | | |
| C3 | C1 | | | | | | |
| C4 | C1 | | | | | | |
| C5 | C1 | | | | | | |
| C6 | | CAP,MICA | 15PF | 5% | 500V | 2260014-00 | 1 |
| C7 | C1 | | | | | | |
| C8 | C1 | | | | | | |
| C9 | | CAP,CER | 220PF | 10% | 100V | 2150047-00 | 1 |
| C10 | C1 | | | | | | |
| C11 | C1 | | | | | | |
| C12 | | CAP,ML,NPO | 390PF | 5% | 50V | 2350047-00 | 1 |
| C13 | C1 | | | | | | |
| C14 | C1 | | | | | | |
| C15 | C1 | | | | | | |
| C16 | C1 | | | | | | |
| C17 | C1 | | | | | | |
| C18 | | CAP,DISC,CER | .1µF | | 50V | 2150092-00 | 1 |
| C19 | C1 | | | | | | |
| C20 | C1 | | | | | | |
| C21 | | CAP,TANTALUM | 33µF | 20% | 10V | 2300015-00 | 3 |
| C22 | C1 | | | | | | |
| C23 | C1 | | | | | | |
| C24 | C1 | | | | | | |
| C25 | C1 | | | | | | |
| C26 | C1 | | | | | | |
| C27 | C1 | | | | | | |
| C28 | C1 | | | | | | |
| C29 | C1 | | | | | | |
| C30 | C1 | | | | | | |
| C31 | | CAP,TANTALUM | 10µF | 20% | 25V | 2300029-00 | 4 |
| C32 | C31 | | | | | | |
| C33 | C31 | | | | | | |
| C34 | C1 | | | | | | |
| C35 | C21 | | | | | | |
| C36 | C31 | | | | | | |
| C37 | C21 | | | | | | |
| C38 | C1 | | | | | | |
| C39 | C1 | | | | | | |
| C40 | C1 | | | | | | |
| C41 | C1 | | | | | | |
| C42 | C1 | | | | | | |
| C43 | | CAP,TANTALUM | 100µF | 20% | 6.3V | 2300024-00 | 1 |
| C44 | C1 | | | | | | |
| C45 | | CAP,ML,NPO | 1000PF | 5% | 50V | 2350046-00 | 5 |
| C46 | C1 | | | | | | |
| C47 | C1 | | | | | | |
| C48 | C45 | | | | | | |
| C49 | C45 | | | | | | |
| C50 | C45 | | | | | | |
| C51 | C1 | | | | | | |
| C52 | C1 | | | | | | |
| C53 | C1 | | | | | | |
| C54 | C45 | | | | | | |
| CR1 | | DIODE,1N5234,ZENER 6.2V | | | | 2705234-00 | 1 |
| J1 | | NOT USED | | | | | |
| J2 | | CONN,COAX PC RCPT,SNAP NANOHEX | | | | 2610038-00 | 4 |
| J3 | J2 | | | | | | |
| J4 | J2 | | | | | | |
| J5 | J2 | | | | | | |

## A6 COUNT CHAIN/GATE (Continued) 2020421-03 Rev. B

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| L1 | | INDUCTOR,1.0µH | | | | 3510003-00 | 1 |
| L2 | | INDUCTOR,.068µH,REF CHK | | | | 3520017-00 | 1 |
| L3 | | INDUCTOR,5.6µH | | | | 3510036-00 | 1 |
| Q1 | | XSTR,2N4126,PNP,GP | | | | 4704126-00 | 3 |
| Q2 | Q1 | | | | | | |
| Q3 | | XSTR,2N4124,NPN,GP | | | | 4704124-00 | 4 |
| Q4 | Q3 | | | | | | |
| Q5 | Q3 | | | | | | |
| Q6 | Q3 | | | | | | |
| Q7 | Q1 | | | | | | |
| Q8 | | XSTR,NE02137,NPN,MICROWAVE | | | | 4710032-00 | 4 |
| Q9 | Q8 | | | | | | |
| Q10 | | XSTR,MMBT3960,NPN SWITCHING | | | | 1410101-00 | 1 |
| Q11 | | XSTR,MRF536,PNP,RF | | | | 4710044-00 | 2 |
| Q12 | Q8 | | | | | | |
| Q13 | Q11 | | | | | | |
| Q14 | Q8 | | | | | | |
| R1 | | RES,M/OX | 2.21K | 1/8W | 1% | 4062211-00 | 3 |
| R2 | | RES,M/OX | 4.75K | 1/8W | 1% | 4064751-00 | 6 |
| R3 | | RES,M/OX | 511 | 1/8W | 1% | 4065110-00 | 3 |
| R4 | R2 | | | | | | |
| R5 | R1 | | | | | | |
| R6 | | RES,M/OX | 221 | 1/10W | 1% | 4052210-00 | 2 |
| R7 | R3 | | | | | | |
| R8 | R6 | | | | | | |
| R9 | | RES,M/OX | 301 | 1/8W | 1% | 4063010-00 | 1 |
| R10 | | RES,M/OX | 10.0 | 1/8W | 1% | 4061009-00 | 3 |
| R11 | | RES,M/OX | 2.00K | 1/8W | 1% | 4062001-00 | 2 |
| R12 | | RES,M/OX | 619 | 1/10W | 1% | 4056190-00 | 2 |
| R13 | | RES,M/OX | 1K | 1/8W | 1% | 4061001-00 | 11 |
| R14 | R10 | | | | | | |
| R15 | R12 | | | | | | |
| R16 | | RES,M/OX | 27.4 | 1/10W | 1% | 4052749-00 | 1 |
| R17 | | RES,M/OX | 200 | 1/8W | 1% | 4062000-00 | 1 |
| R18 | R13 | | | | | | |
| R19 | R11 | | | | | | |
| R20 | R1 | | | | | | |
| R21 | | RES,M/OX | 332 | 1/8W | 1% | 4063320-00 | 4 |
| R22 | R2 | | | | | | |
| R23 | R2 | | | | | | |
| R24 | R2 | | | | | | |
| R25 | | RES,M/OX | 2.74K | 1/10W | 1% | 4052741-00 | 1 |
| R26 | R2 | | | | | | |
| R27 | | RES,M/OX | 39.2 | 1/10W | 1% | 4053929-00 | 3 |
| R28 | | RES,M/OX | 10.0K | 1/8W | 1% | 4061002-00 | 6 |
| R29 | R28 | | | | | | |
| R30 | | RES,M/OX | 1.82K | 1/8W | 1% | 4061821-00 | 1 |
| R31 | R13 | | | | | | |
| R32 | | RES,M/OX | 750K | 1/4W | 2% | 4130754-00 | 1 |
| R33 | R13 | | | | | | |
| R34 | R13 | | | | | | |
| R35 | R13 | | | | | | |
| R36 | | RES,M/OX | 90.9 | 1/10W | 1% | 4059099-00 | 1 |
| R37 | | RES,M/OX | 20.0K | 1/8W | 1% | 4062002-00 | 4 |
| R38 | R37 | | | | | | |
| R39 | R28 | | | | | | |
| R40 | R28 | | | | | | |
| R41 | R28 | | | | | | |
| R42 | R37 | | | | | | |
| R43 | R37 | | | | | | |

## A6 COUNT CHAIN/GATE (Continued) 2020421-03 Rev. B

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| R44 | R13 | | | | | | |
| R45 | R13 | | | | | | |
| R46 | | RES,M/OX | 3.01K | 1/8W | 1% | 4063011-00 | 1 |
| R47 | R13 | | | | | | |
| R48 | | RES,M/OX | 130.0 | 1/8W | 1% | 4061300-00 | 2 |
| R49 | | RES,M/OX | 82.5 | 1/10W | 1% | 4058259-00 | 2 |
| R50 | R27 | | | | | | |
| R51 | R10 | | | | | | |
| R52 | R27 | | | | | | |
| R53 | | RES,M/OX | 47.5 | 1/8W | 1% | 4064759-00 | 1 |
| R54 | R28 | | | | | | |
| R55 | R21 | | | | | | |
| R56 | | RES,M/OX | 51.1 | 1/8W | 1% | 4065119-00 | 2 |
| R57 | R21 | | | | | | |
| R58 | R21 | | | | | | |
| R59 | | RES,M/OX | 274 | 1/8W | 1% | 4062740-00 | 1 |
| R60 | R13 | | | | | | |
| R61 | R56 | | | | | | |
| R62 | | RES,M/OX | 100 | 1/8W | 1% | 4061000-00 | 1 |
| R63 | R13 | | | | | | |
| R64 | R48 | | | | | | |
| R65 | R49 | | | | | | |
| R66 | | RES,M/OX | 487 | 1/10W | 1% | 4054870-00 | 2 |
| R67 | | RES,CC | 5.6 | 1/4W | 5% | 4010569-00 | 3 |
| R68 | R66 | | | | | | |
| R69 | | RES,M/OX | 56.2 | 1/8W | 1% | 4065629-00 | 2 |
| R70 | R69 | | | | | | |
| R71 | R67 | | | | | | |
| R72 | R67 | | | | | | |
| R73 | R3 | | | | | | |
| TP1 | | NOT USED | | | | | |
| TP2 | | NOT USED | | | | | |
| TP3 | | NOT USED | | | | | |
| TP4 | | NOT USED | | | | | |
| TP5 | | NOT USED | | | | | |
| TP6 | | NOT USED | | | | | |
| TP7 | | NOT USED | | | | | |
| TP8 | | NOT USED | | | | | |
| U1 | | IC,74LS132 | | | | 3084132-00 | 1 |
| U2 | | IC,74ACT00PC | | | | 3110011-00 | 1 |
| U3 | | IC,MK5009N,P-CHANNEL MOS DIVIDER | | | | 3035009-00 | 1 |
| U4 | | IC,74LS490 | | | | 3084490-00 | 1 |
| U5 | | IC,74LS175 | | | | 3084175-00 | 1 |
| U6 | | IC,74LS74 | | | | 3087474-00 | 2 |
| U7 | | IC,74F02 | | | | 3060011-00 | 1 |
| U8 | U6 | | | | | | |
| U9 | | IC,MC10131L,DUAL,M-S FF | | | | 3110131-00 | 1 |
| U10 | | IC,74LS196 | | | | 3084196-00 | 1 |
| U11 | | IC,74LS160 | | | | 3084160-00 | 1 |
| U12 | | IC,74LS04 | | | | 3087404-00 | 1 |
| U13 | | IC,LS7031,CNTR,6-DECADE,UP,PMDS | | | | 3057031-00 | 1 |
| U14 | | IC,MC68B21P,PRPHL INTERFACE ADAPTER | | | | 3086821-00 | 1 |
| U15 | | IC,10125,ECL 10K,TRANSLATORS | | | | 3110125-00 | 1 |
| U16 | | IC,555,TIMER | | | | 3040555-00 | 1 |
| U17 | | IC,LM741C,OP AMP | | | | 3040741-00 | 1 |
| U18 | | IC,SP8637B,HIGH SPEED DIVIDERS/10 | | | | 3010637-00 | 1 |
| U19 | | IC,10H116,ECL 10KHZ,LINE RCVR | | | | 3118116-00 | 1 |
| XU1 | | NOT USED | | | | | |
| XU2 | | NOT USED | | | | | |

## A6 COUNT CHAIN/GATE (Continued) 2020421-03 Rev. B

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| XU3 | | NOT USED | | |
| XU4 | | NOT USED | | |
| XU5 | | NOT USED | | |
| XU6 | | NOT USED | | |
| XU7 | | NOT USED | | |
| XU8 | | NOT USED | | |
| XU9 | | NOT USED | | |
| XU10 | | NOT USED | | |
| XU11 | | NOT USED | | |
| XU12 | | NOT USED | | |
| XU13 | | CONN,SOCKET,DIP,40 PIN | 2630022-00 | 2 |
| XU14 | XU13 | | | |
| XU15 | | NOT USED | | |
| XU16 | | NOT USED | | |
| XU17 | | NOT USED | | |
| XU18 | | NOT USED | | |
| Y1 | | OSC,TCXO | 2030002-00 | 1 |
| HARDWARE USED IN THIS ASSEMBLY | | | | |
| | | HANDLE,PCB | 5230001-00 | 2 |
| | | PIN,ROLL,3/32 DIA 1/4 LG | 5110008-00 | 2 |
| | | WIRE,INSUL,30AWG,GREEN | 5430555-00 | 1 |
| | | PCB SCHEMATIC DIAGRAM | 5500421-03 C | REF. |

Count Chain/Gate Component Locator
(PCB Assembly A6)

(See following page)

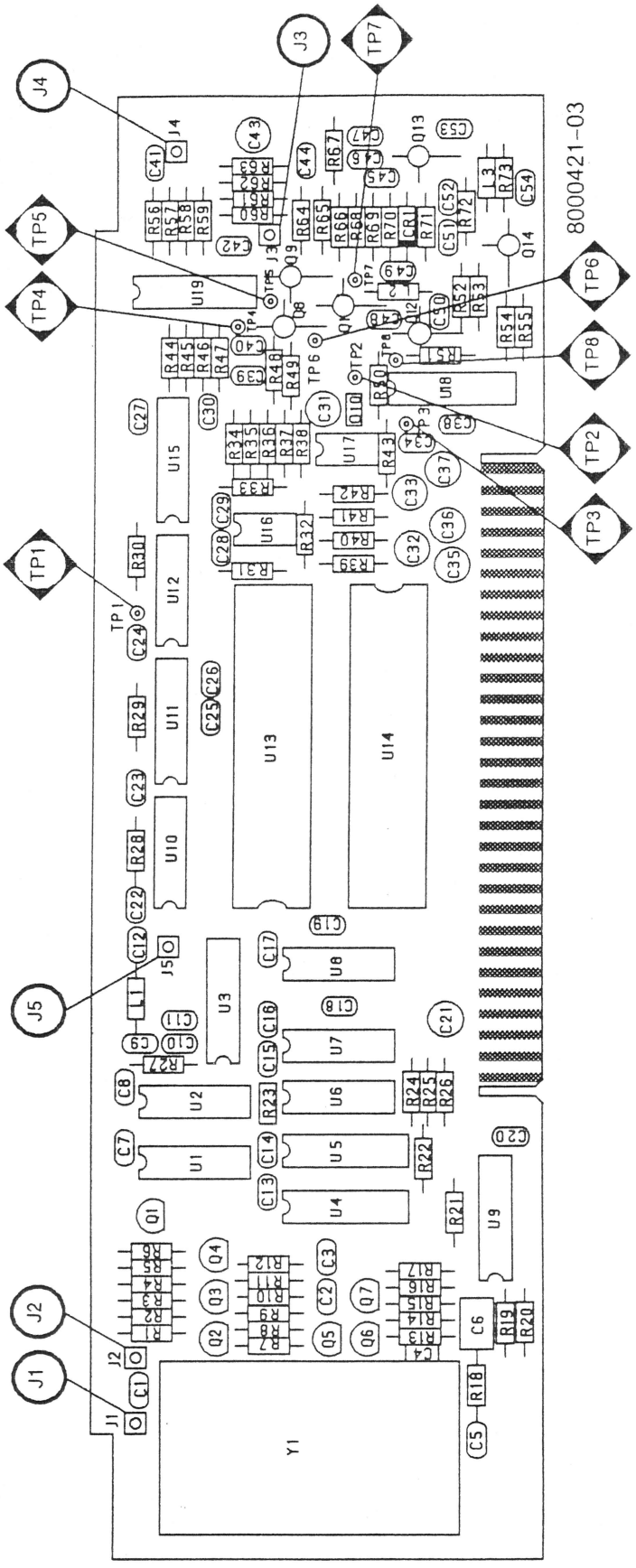
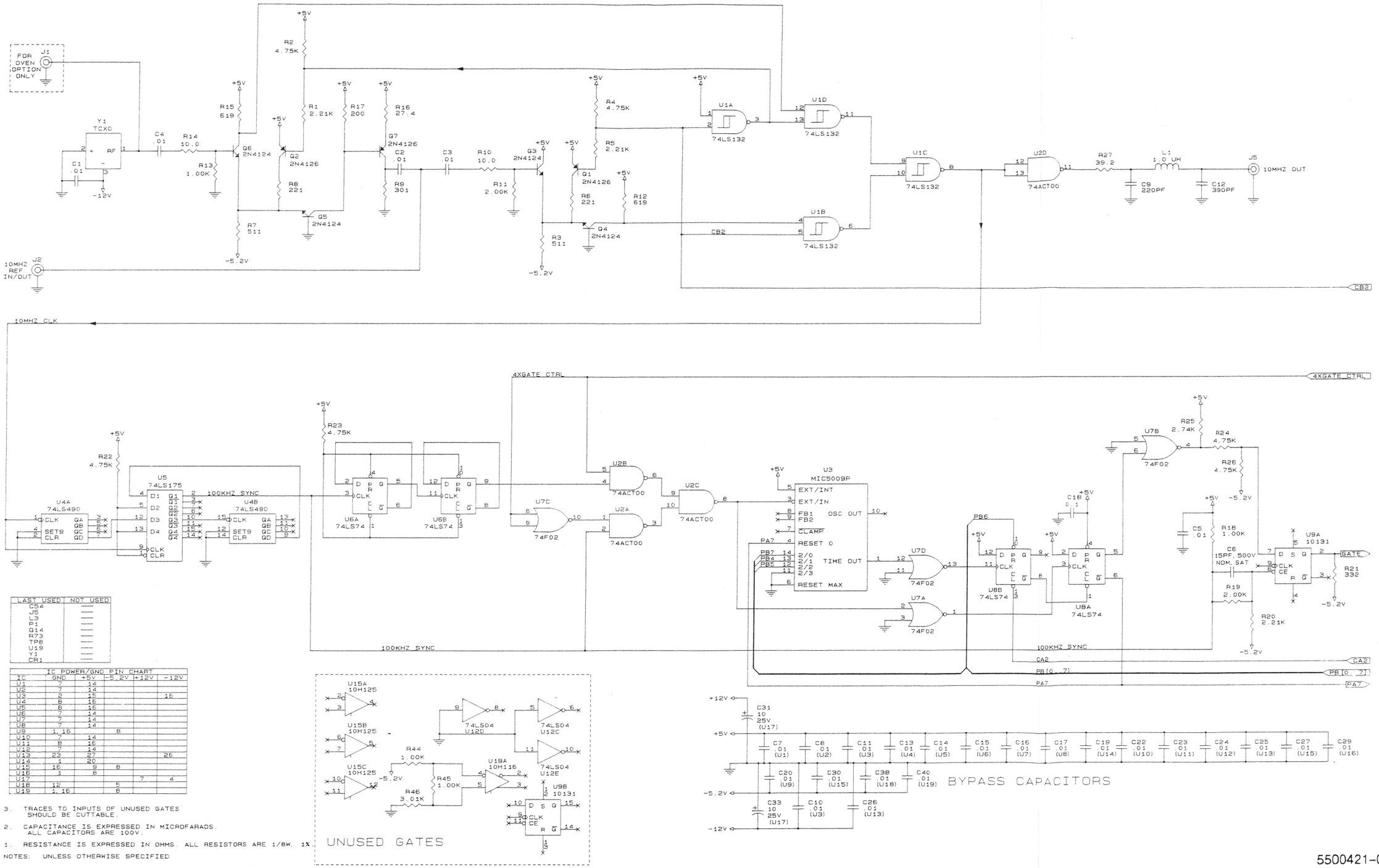



Figure 10-18. Count Chain/Gate (A6) Component Locator.




| LAST USED | NOT USED |
|---|---|
| C54 | |
| U5 | |
| L3 | |
| P1 | |
| Q14 | |
| R73 | |
| TP8 | |
| U19 | |
| Y1 | |
| CR1 | |

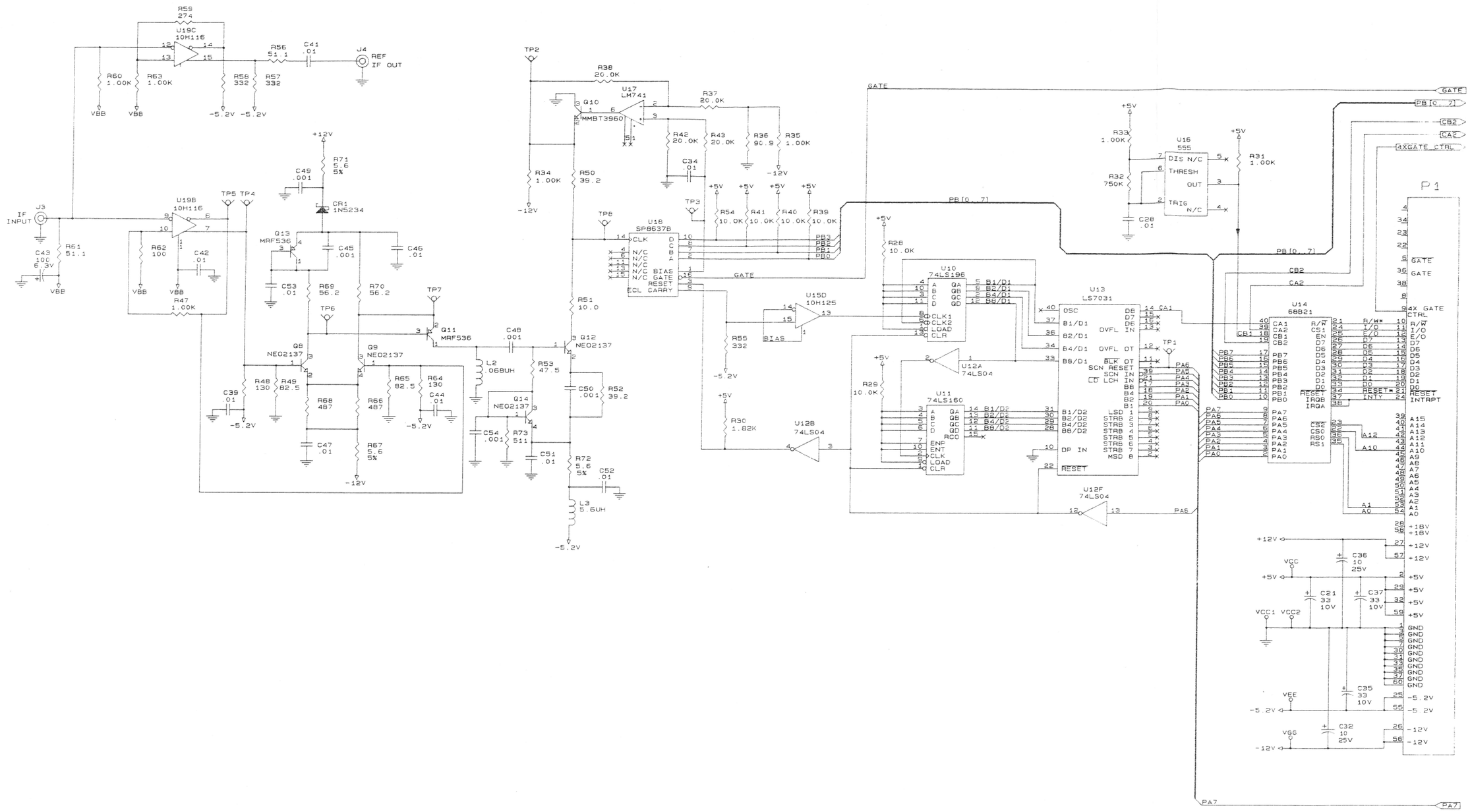
| IC | IC POWER/GND PIN CHART GND | +5V | -5.2V | +12V | -12V |
|---|---|---|---|---|---|
| U1 | 7 | 14 | | | |
| U2 | 7 | 14 | | | |
| U3 | 2 | 15 | | | 16 |
| U4 | 8 | 16 | | | |
| U5 | 8 | 16 | | | |
| U6 | 7 | 14 | | | |
| U7 | 7 | 14 | | | |
| U8 | 7 | 14 | | | |
| U9 | 1, 16 | | 8 | | |
| U10 | 7 | 14 | | | |
| U11 | 8 | 16 | | | |
| U12 | 7 | 14 | | | |
| U13 | 23 | 27 | | | 26 |
| U14 | 1 | 20 | | | |
| U15 | 16 | 9 | 8 | | |
| U16 | 1 | 8 | | | |
| U17 | | | | 7 | 4 |
| U18 | 12 | | 5 | | |
| U19 | 1, 16 | | 8 | | |

3. TRACES TO INPUTS OF UNUSED GATES SHOULD BE CUTTABLE.
2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 100V.
1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W, 1%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500421-03

**Figure 10-19. Count Chain/Gate (A6 Schematic Diagram. (Sheet 1 of 2)**




5500421-0

**Figure 10-19. Count Chain/Gate (A Schematic Diagram (Sheet 2 of 2)**

# A9
# SIGNAL CONDITIONER
# (2020420-03)

The Signal Conditioner assembly processes signals from all three bands, along with the self-test signal, and converts the selected signal into an ECL signal before being applied to the Count Chain/Gate generator assembly (A6) to be counted. Since the exact function varies depending on the input selected, a functional description for self-test and each of the various bands is provided.

## SELF-TEST

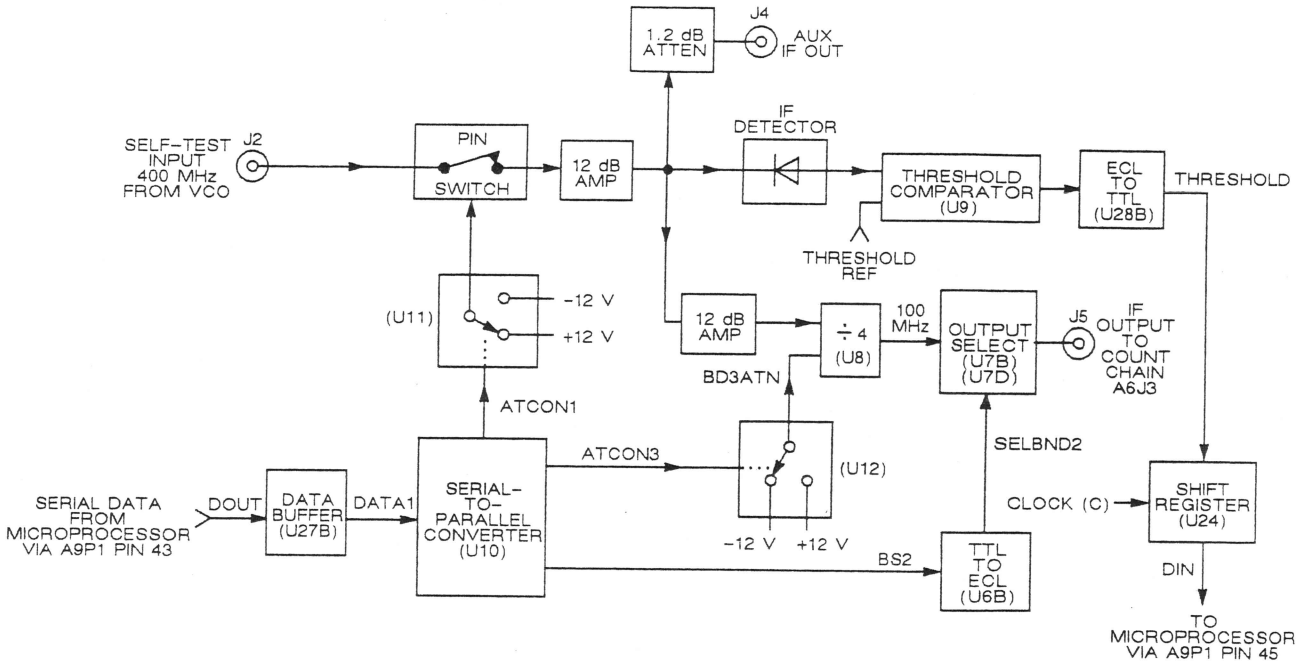



**Figure 10-20. Signal Conditioner Functional Block Diagram for Self-Test Mode.**

In the self-test mode, the input at J2 is a 400 MHz sine wave, at approximately -10 dBm, generated by the phase-locked VCO in the A10 assembly. This signal is passed through the PIN switch (CR4 and CR5) and amplifiers U5 and U4, to the divide-by-four IC, U8. The output of U8, 100 MHz in self-test, is gated through U7B and U7D to J5, the IF output to the A6 Count Chain/Gate assembly.

When the self-test mode is initiated, the microprocessor goes through a series of steps. The first step is to set the phase-locked VCO to 400 MHz. Next, the microprocessor sends, in the form of serial data, the commands necessary to set up the Signal Conditioner for the self-test mode.

The serial data is received at A9 on pin 43 of the edge connector (P1) as DOUT. The data passes through the constantly enabled line buffer (U27B) where the signal becomes DATA1. This signal (DATA1) is then routed to U10 pin 14 where it is converted from serial data to parallel data. The serial clock on U10 pin 11 (C), clocks the data in and the signal at pin 12 (STRB4) loads the output latches with the parallel data. The parallel data is applied to the TTL to ECL translators U6A through U6D and to analog switches U11 and U12. In the self-test mode, U10 pins 2 and 4 are TTL high and the remaining outputs are low.

The high output from U10 pin 4 is connected to the analog switch U11 at pin 15 closing the switch between pins 1 and 16, and opening the switch between pins 3 and 4. This causes the output on U11 pins 1 and 3 to be +12 Vdc causing the signal from J2 to pass through the pin switch, consisting of diodes CR4 and CR5.

The low output from U10 pin 6 is connected to the analog switch U12 at pin 15 opening the switch between pins 1 and 16, and closing the switch between pins 3 and 4. This causes the output on U12 pins 1 and 3 to be -12 Vdc. The -12 Vdc enables U8, the divide-by-four.

The high output from U10 pin 2 is passed through the TTL to ECL translator (U6B) to U7B pin 9. This enables the 100 MHz signal at U7B pin 8 to pass though U7B, through U7D and out J5, to the IF input on A6, the Count Chain/Gate generator assembly.

## BAND 1

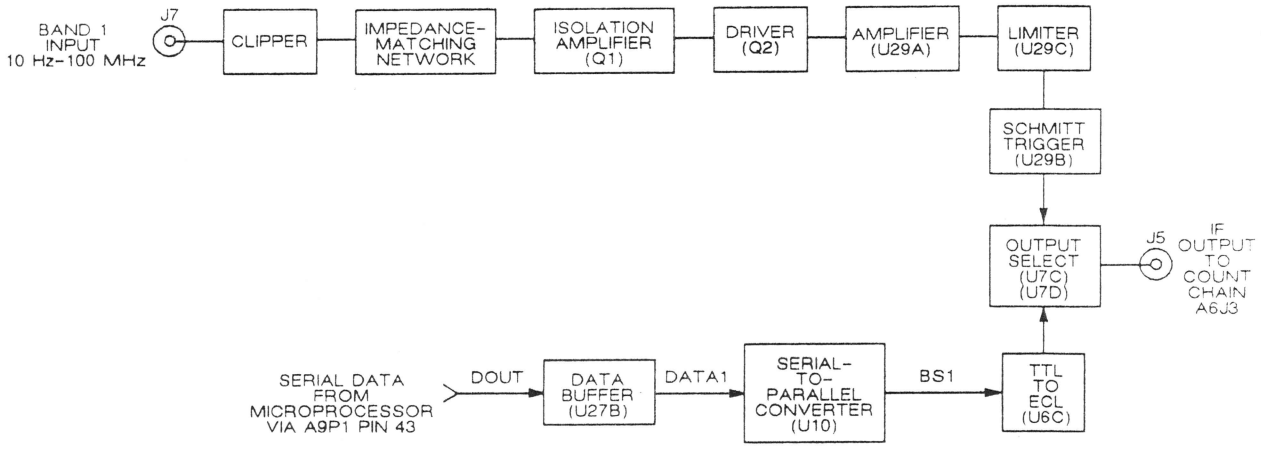



**Figure 10-21. Signal Conditioner Functional Block Diagram for Band 1.**

During Band 1 operation the Signal Conditioner converts the Band 1 input signal at J7 into an ECL signal and routes it to J5, the IF output to the A6 Count Chain assembly. The IF threshold circuit is disabled in this band and the counter continuously generates the gate signals for the count chain.

The Band 1 input signal (10 Hz to 100 MHz) from the front panel is directly connected to J7 on the Signal Conditioner. The amplitude of the input signal is limited to ±0.7 volts by CR15 and CR16. The impedance matching network in conjunction with Q1, the FET isolation amplifier, provides the 1 megohm input impedance. The signal from the source of Q1 is fed to Q2, a driver/current amplifier. The output from Q2 is ac coupled to amplifier U29A which is primarily used to amplify the lower level signals. The output of U29A is fed to the limiter U29C. The combination of U29A and U29C flattens the peaks of the input signal, providing a nearly constant amplitude output over the dynamic range of Band 1, at the input to U29B. The positive feedback on U29B, by R107, reduces the rise and fall time of the input signal from U29C, providing a sharp-edged square wave at U29B pin 9. The sharp edges on the output signal, at TP14, minimize the potential of false triggering due to noise.

When Band 1 is selected, the microprocessor sends, in the form of serial data, the commands necessary to set up the Signal Conditioner for Band 1 operation. The serial data is received at P1 pin 43 as DOUT. The data passes through the constantly enabled line buffer (U27B), where the signal becomes DATA1. This signal (DATA1) is then routed to U10 pin 14 where it is converted from serial

data to parallel data. The serial clock on U10 pin 11 (C) clocks the data in, and the signal at pin 12 (STRB4) loads the output latches with the parallel data. The parallel data is applied to the TTL to ECL translators U6A through U6D and to analog switches U11 and U12. When Band 1 is selected, U10 pins 1, 5, and 6 are TTL high, and the remaining outputs are low.

The high output from U10 pin 6 is connected to the analog switch U12 at pin 15 closing the switch between pins 1 and 16, and opening the switch between pins 3 and 4. This causes the output on U12 pins 1 and 3 to be +12 Vdc. The +12 Vdc disables divide-by-four U8.

The high output from U10 pin 5 is converted from TTL to ECL by U6D. The signal is inverted to an ECL low (-1.8 V) by U6D and is connected to U9 pin 6, the threshold detector control line. The ECL low (-1.8 V) disables U9, preventing the threshold detector from toggling during Band 1 operation.

The high output from U10 pin 1 is converted from TTL to ECL by U6C. The resulting ECL high (-0.8 V) is connected to U7C pin 14. This enables the Band 1 signal at U7C pin 13 to pass through U7C through U7D, and out J5, to the IF input on A6, the Count Chain/Gate generator assembly.

## BAND 2

The function of the Signal Conditioner during Band 2 operation will be described by dividing it into the following functional blocks:

- Input amplifier
- Threshold detector
- AGC loop
- Prescaler
- Output selector

### INPUT AMPLIFIER

The Band 2 input signal (100 MHz to 1 GHz) from the front panel is directly connected to J1 on the Signal Conditioner. A 6.6 dB T-pad at the input, consisting of R1, R2, and R3, provides the 50 ohm input impedance. The output from the T-pad connects to a 65 MHz high pass filter, consisting of C3, C4, and L2, which blocks any low frequency signals present at the Band 2 input.

The Band 2 signal is then amplified by approximately 12 dB by U1, and applied to a pin attenuator consisting of CR1, CR2, CR3 and the associated circuitry. The attenuation of the pin attenuator is controlled by an automatic gain control (AGC) loop. The output of the pin attenuator is fed to U2, which amplifies the signal by approximately 12 dB. The output of U2 is fed to U3 which further amplifies the signal by approximately 20 dB.

The output of U3 is fed to the Band 2 PIN switch, consisting primarily of CR7, CR8, and CR9. The PIN switch blocks the Band 2 signal whenever Band 2 is not selected. The control signal for the PIN switch comes from U12 pins 6 and 8. A +12 V signal from U12 pins 5 and 6 causes the Band 2 signal to pass through the PIN switch. The output from the PIN switch is connected to U5 which provides another 12 dB of amplification. A portion of the output signal from U5 is capacitively coupled to both the auxiliary IF output at J4 and the threshold detector. The main portion of the signal passes through R30, which serves as a 3 dB attenuator, and is capacitively coupled to U4, which provides an additional 12 dB of amplification. The output of U4 is capacitively coupled to U8, the divide-by-four prescaler.

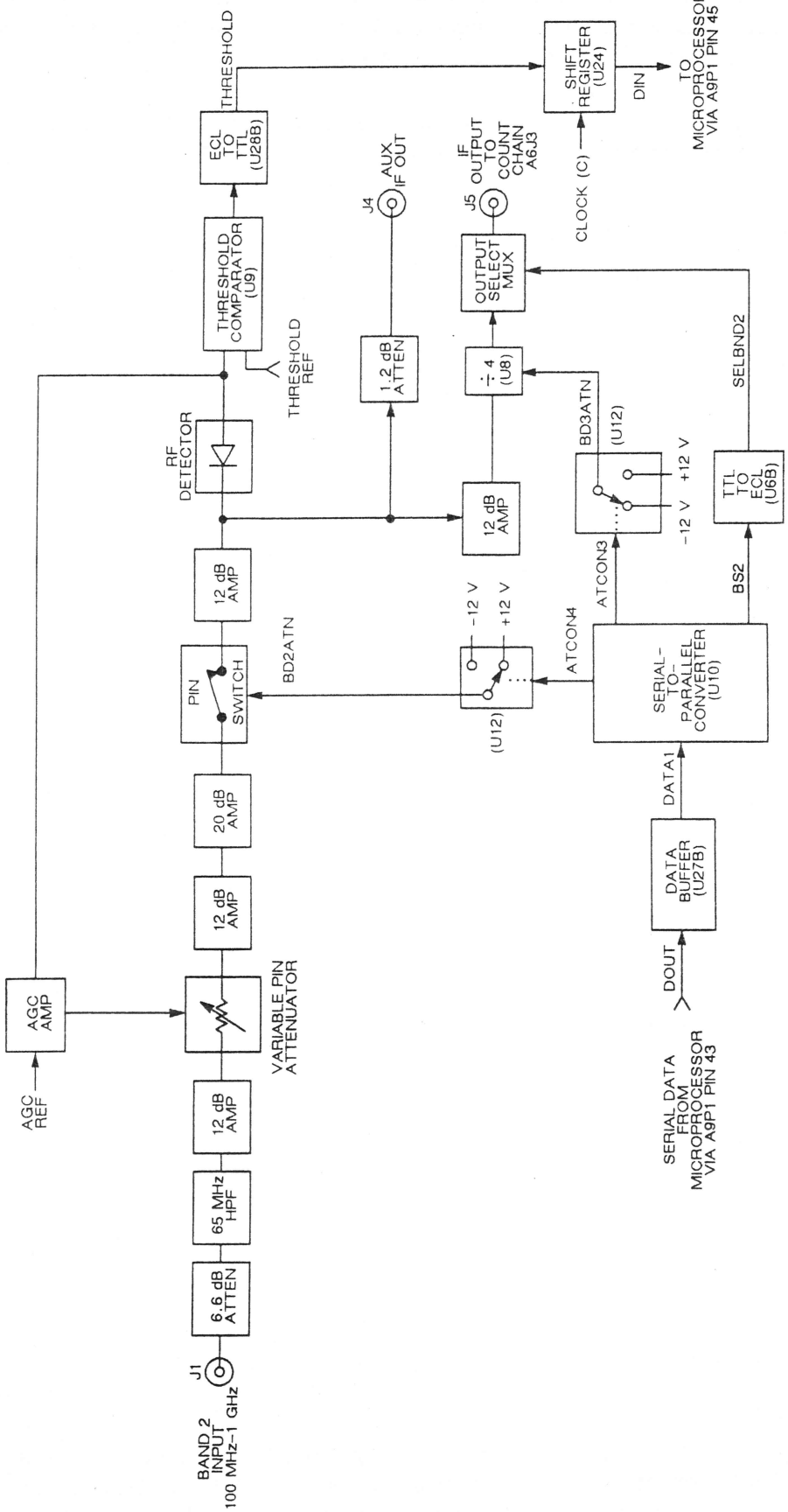



**Figure 10–22. Signal Conditioner Functional Block Diagram for Band 2.**

## THRESHOLD DETECTOR

The threshold detector performs two functions. The first is to generate a dc voltage level proportional to the input signal level, and the second is to provide a digital signal which is true whenever the input signal is above threshold.

The RF detector provides a dc voltage level proportional to the input signal level, and provides the input for both the AGC loop and the threshold comparator. The RF detection is performed by CR10, a hot carrier diode which is biased at approximately -0.3 volts by R41 and R42. The biasing improves the temperature stability of the detector, and increases the detector's sensitivity on low level signals. The output of CR10 is applied to a 100 kHz low pass filter to eliminate unwanted high frequency signals.

A high speed comparator, consisting of U9 and the associated circuitry, is the source of the digital threshold signal. This signal is true whenever a signal above a preset reference level is applied to the input at U9 pin 4. The reference level on U9 pin 3 is set to approximately -52 mV by voltage divider R57 and R58. Whenever the signal at U9 pin 4 is greater than the reference level the output at U9 pin 11 goes to an ECL high (-.8 V) and the output at U9 pin 12 goes to an ECL low (-1.8 V). The differential output from the high speed comparator is applied to U28B, which converts it from a differential ECL signal into a single-ended TTL signal.

The TTL threshold signal from U28B pin 7 is applied as a serial input to U24. During Band 2 operation, a clock signal at U24 pin 2, continuously shifts in the serial data from U24 pin 10. The output from U24 at pin 9 is monitored by the microprocessor and will go high whenever a Band 2 input signal above threshold is detected. The microprocessor responds by enabling gate generation which begins the measurement cycle.

## AGC LOOP

The AGC Loop adjusts the attenuation of the Band 2 signal to maintain a constant signal amplitude at the output of U5. The AGC Loop samples a portion of the detected RF signal, at TP7, and applies it to comparator U14. The voltage reference for the comparator is set by resistors R64 and R66. An increase in RF level from U5 pin 3 causes the detected RF level, at TP7, to increase in a negative direction. The signal from TP7 is applied to the voltage comparator. As the input voltage to the comparator increases in a negative direction the output voltage from the comparator, at U14 pin 6, also increases in a negative direction increasing the attenuation of the pin attenuator. The output voltage from the comparator ranges from -1 Vdc for maximum attenuation to +11 Vdc for minimum attenuation.

## PRESCALER

The prescaler, U8, is a high speed ECL divider with a constant divide ratio of 4. During Band 2 operation the prescaler is enabled by a -11.3 V signal applied to U8 pin 3. The Band 2 RF signal is applied to U8 pin 2, and will range from 100 MHz to 1 GHz. The output signal, the Band 2 IF signal, at U8 pin 6, will range between 25 MHz to 250 MHz.

## OUTPUT SELECTOR

When Band 2 is selected, U10 pins 2 and 7 are TTL high, and the remaining outputs are low. The high output from U10 pin 7 is connected to the analog switch U12 at pin 10, closing the switch between pins 8 and 9, and opening the switch between pins 5 and 6. This causes the output on U12 pins 6 and 8 to go to +12 Vdc.

The +12 Vdc is the control voltage for the Band 2 pin switch, consisting primarily of diodes CR7, CR8, and CR9. The +12 Vdc causes the pin switch to pass the signal to amplifiers U5 and U4. The output of U4 supplies the RF input to U8, the divide-by-four. During Band 2 operation, U8 is enabled by a

-11.3 V signal on U8 pin 3. The IF output at U8 pin 6 is an ECL signal with a frequency equal to the input frequency divided by four.

During Band 2 operation, the IF signal from U8 pin 6 is applied to U7B pin 8. A high output from U10 pin 2 is converted from ECL to TTL by U6B. The ECL high output at U6B pin 2 is applied to U7B pin 9. This enables the Band 2 IF signal at U7B pin 8 to pass through U7B, through U7D and out J5. The signal at J5 connects to the IF input on A6, the Count Chain/Gate generator assembly.

## BAND 3

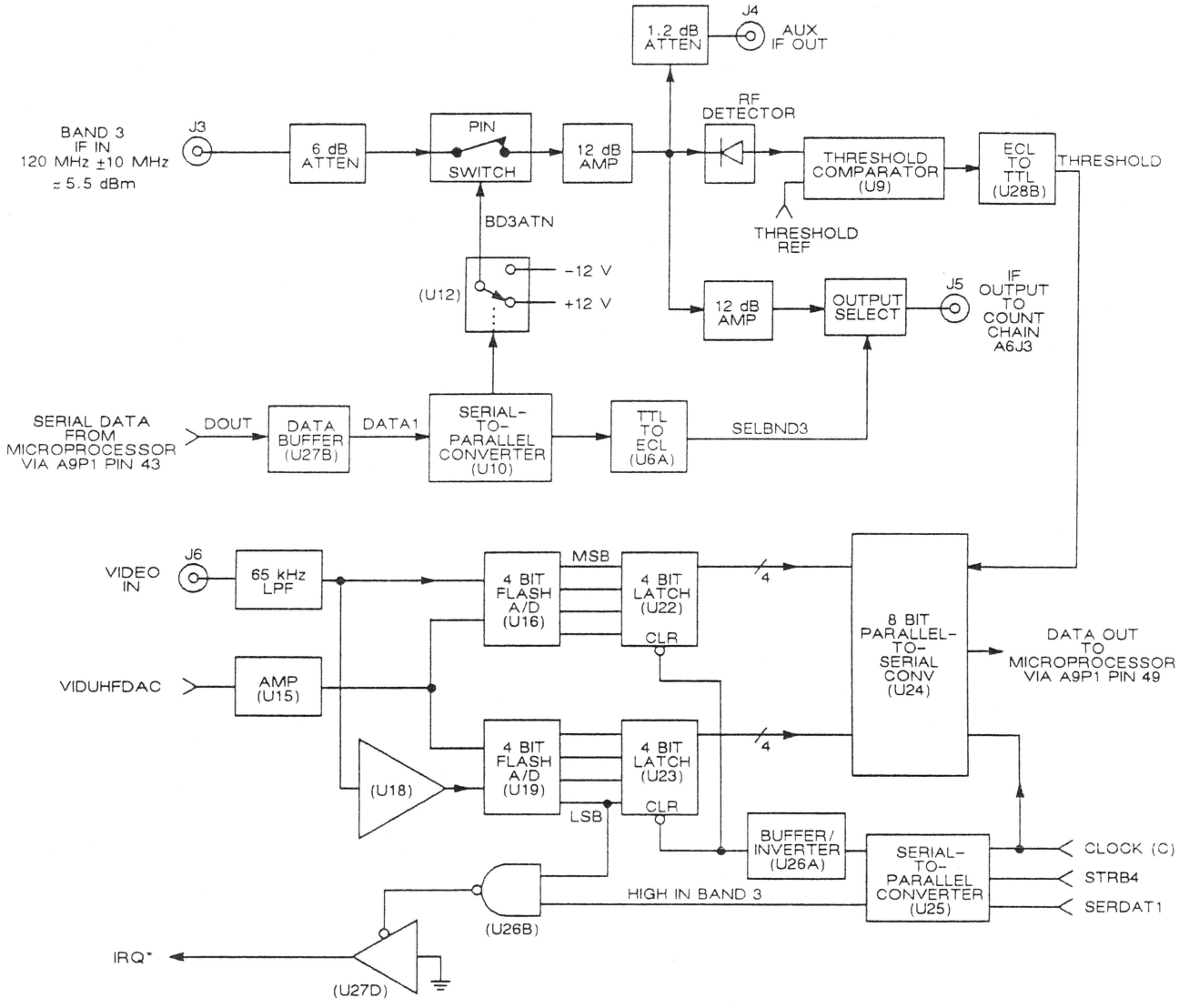



**Figure 10-23. Signal Conditioner Functional Block Diagram for Band 3.**

The function of the Signal Conditioner during Band 3 operation will be described by dividing it into the following functional blocks:

- Signal amplitude determination
- Input amplifier
- IF threshold detector
- Output selector

## SIGNAL AMPLITUDE DETERMINATION

To measure signals in the microwave band it is first necessary to determine their amplitude. During this process the local oscillator is turned off and the microwave mixer, at the output of the YIG filter, is used as a detector. The output from the mixer is applied as the video signal to J6 of the Signal Conditioner. The Signal Conditioner continuously converts the video input signal into a 16-bit digital word with a value proportional to the amplitude of the microwave signal. This data is used by the microprocessor to determine the largest signal present and to center the YIG filter on the input signal.

The video signal, from J6, is first routed through a 65 kHz low pass filter consisting of C55, L10 and C61, to eliminate unwanted noise. The signal is then applied to a flash analog to digital conversion circuit consisting of eight comparators arranged in two sets of four (U16, U17, U19 and U20). During the RF search routine, the comparator voltage levels are set approximately 6 dB apart by resistive voltage dividers.

The voltage reference for the A/D is controlled by the microprocessor via DAC U13. The STRB5 signal from address decoder U21 pin 19 is connected to U13 pin 6 and remains active while the serial data at U13 pin 7 is clocked into U13 by the clock on U13 pin 5. The voltage reference from U13 is buffered by U15 prior to being applied to the voltage dividers.

During the RF search routine the YIG filter is swept across the band. The LSB of the flash A/D is applied to the AND gate U26B at pin 5. The other input to the AND gate at pin 4 is high in Band 3. If a signal is found the LSB from the flash A/D will go high, causing the output from U26B to go low. The low output from U26B pin 6 connects to U27D pin 13 which causes the output from U27D pin 11 to go low. The output from U27D pin 11 is an interrupt line to the microprocessor.

The outputs of the A/D converters are applied to 4-bit latches U22 and U23. These latches hold the A/D output data until they are reset by the microprocessor through shift register U25 and inverter U26A. Provided a video signal of sufficient amplitude is present, the latch outputs are then applied to U24, an 8-bit parallel-to-serial converter. The microprocessor reads the digital information, via the DIN line from pin 9 of U24, by shifting one bit at a time through U24.

As the YIG is swept across the band any signal found will generate an interrupt to the microprocessor. The microprocessor responds by halting the YIG sweep and reading the data corresponding to the amplitude of the microwave signal. This process continues until all the signals are measured. The microprocessor then selects the largest signal, sets the YIG filter to that frequency, and proceeds to center the YIG filter on the selected signal.

## INPUT AMPLIFIER

The Band 3 IF signal from the Microwave Converter assembly (A10) is connected directly to J3 on the Signal Conditioner. This signal has a frequency of 120 MHz $\pm$10 MHz at approximately 5.5 dBm. A 6 dB T-pad at the input, consisting of R32 and R33, is used for impedance matching. The output from the T-pad connects to a PIN switch consisting primarily of CR11, CR12, and CR6. When Band 3 is selected, the PIN switch control signal (BD3ATN) is at +12 V which allows the Band 3 IF to pass through the PIN switch with minimum attenuation.

The output from the PIN switch is connected to U5, which amplifies the signal by approximately 12 dB. A portion of the output signal from U5 is capacitively coupled to both the auxiliary IF output at J4 and the threshold detector. The main portion of the signal passes through R30, which serves as a 3 dB attenuator, and is capacitively coupled to U4, which provides an additional 12 dB of amplification. The output of U4 is connected to the output select circuit at U7A pin 5 through a series resonant circuit.

## IF THRESHOLD DETECTOR

During Band 3 operation the threshold detector provides a digital signal which is true whenever the IF signal is above threshold. This is accomplished by first detecting the IF signal with a RF detector and then comparing the detected voltage to the threshold reference voltage.

The RF detection is performed by CR10, a hot carrier diode which is biased at approximately -0.3 volts by R41 and R42. The biasing improves the temperature stability of the detector and increases the detector's sensitivity on low level signals. The output of CR10 is applied to a 100 kHz low pass filter to eliminate unwanted high frequency signals.

A high speed comparator, consisting of U9 and the associated circuitry, is the source of the digital threshold signal. This signal is true whenever a signal above a preset reference level is applied to the input at U9 pin 4. The reference level on U9 pin 3 is set to approximately -52 mV by voltage divider R57 and R58. Whenever the signal at U9 pin 4 is greater than the reference level the output at U9 pin 11 goes to an ECL high (-.8 V) and the output at U9 pin 12 goes to an ECL low (-1.8 V). The differential output from the high speed comparator is applied to U28B, which converts it from a differential ECL signal into a single-ended TTL signal.

The TTL threshold signal from U28B pin 7 is applied as a serial input to U24. During Band 3 operation, a clock signal at U24 pin 2 continuously shifts in the serial data from U24 pin 10. The output from U24 at pin 9 is monitored by the microprocessor and will go high whenever a Band 3 input signal above threshold is detected. The microprocessor responds by enabling gate generation which begins the measurement cycle.

## OUTPUT SELECTOR

When Band 3 is selected, U10 pins 3 and 6 are TTL high and the remaining outputs are low. The high output from U10 pin 6 is connected to the analog switch U12 at pin 15, closing the switch between pins 1 and 16, and opening the switch between pins 3 and 4. This causes the output on U12 pins 1 and 3 to go to +12 Vdc.

The +12 Vdc is the control voltage for the Band 3 PIN switch, consisting primarily of diodes CR11, CR12, and CR6. The +12 Vdc causes the PIN switch to pass the signal to amplifiers U5 and U4. The IF output of U4 is connected to NAND gate U7A at pin 5 through a series resonant circuit. A high output from U10 pin 3 is converted from TTL to ECL by U6A. The ECL high output at U6A pin 3 is applied to U7A pin 7. This enables the Band 3 IF signal at U7A pin 5 to pass through U7A, through U7D, and out J5. The signal at J5 connects to the IF input on A6, the Count Chain/Gate generator assembly.

**Table 10-3. Signal Conditioner Control Signals.**

| | SELF-TEST | BAND 1 | BAND 2 | BAND 3 |
|---|---|---|---|---|
| BS1<br>U10 PIN 1 | 0 | 1 | 0 | 0 |
| BS2<br>U10 PIN 2 | 1 | 0 | 1 | 0 |
| BS3<br>U10 PIN 3 | 0 | 0 | 0 | 1 |
| ATCON1<br>U10 PIN 4 | 1 | 0 | 0 | 0 |
| U10 PIN 5 | 0 | 1 | 0 | 0 |
| ATCON3<br>U10 PIN 6 | 0 | 1 | 0 | 1 |
| ATCON4<br>U10 PIN 7 | 0 | 0 | 1 | 0 |
| ATCON2<br>U10 PIN 15 | 0 | 0 | 0 | 0 |
| SLFTST<br>U11 PIN 1, 3 | +12 V | -12 V | -12 V | -12 V |
| BD3ATN<br>U12 PIN 1, 3 | -12 V | +12 V | -12 V | +12 V |
| BD2ATN<br>U12 PIN 5, 6 | -12 V | -12 V | +12 V | -12 V |

NOTE: OUTPUTS FROM U10 ARE TTL LEVELS.

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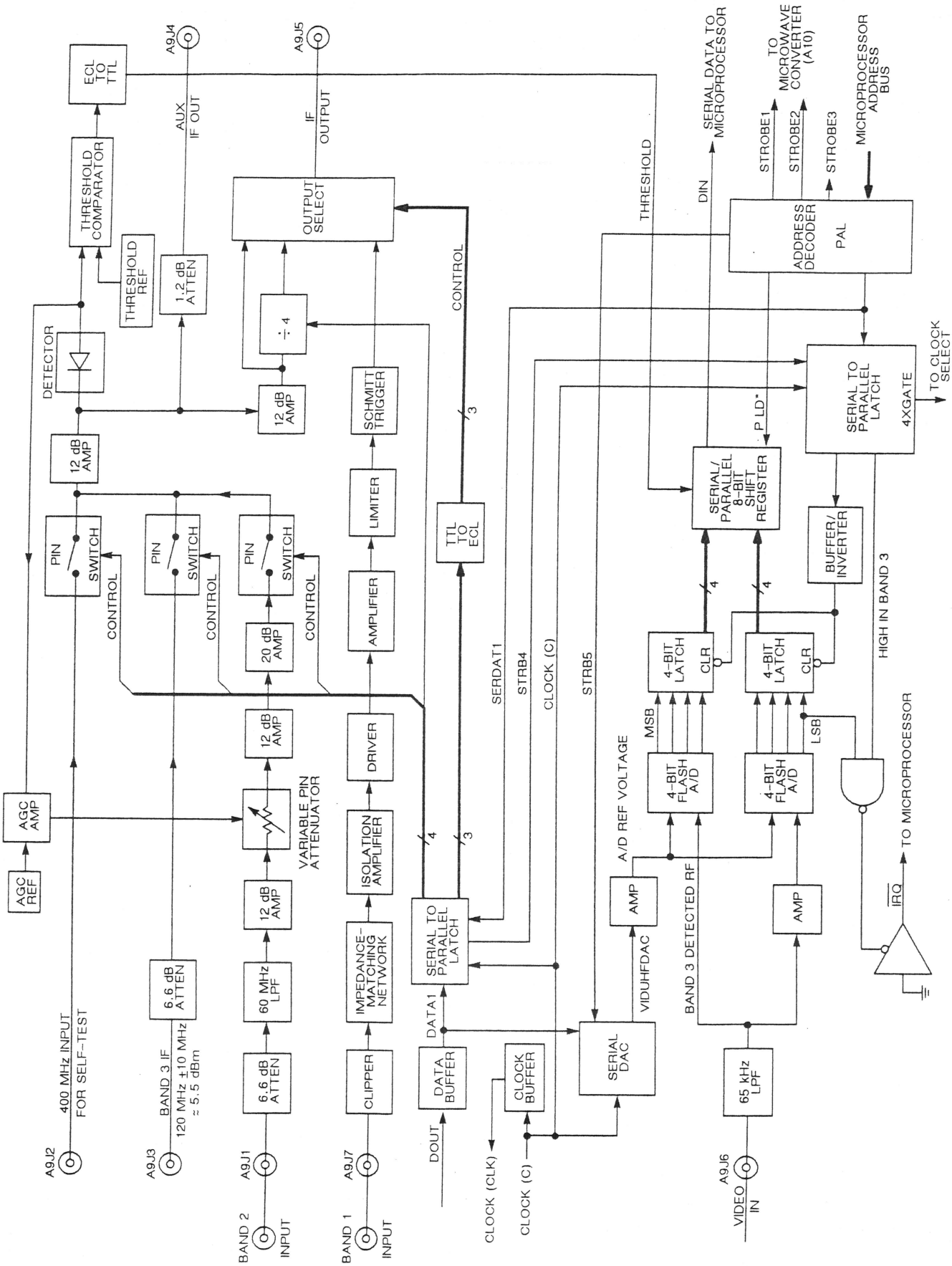


Figure 10-24. Signal Conditioner Functional Block Diagram.

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| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,SMD,Z5U | .1µF | 20% | 50V | 2100046-00 | 57 |
| C2 | | CAP,SMD,CER,NPO | 100PF | 5% | 50V | 2100054-00 | 2 |
| C3 | C2 | | | | | | |
| C4 | | CAP,SMD,CER,NPO | 15PF | 5% | 50V | 2100072-00 | 1 |
| C5 | C1 | | | | | | |
| C6 | C1 | | | | | | |
| C7 | | CAP,SMD,CER,X7R | .001µF | 5% | 50V | 2100037-00 | 16 |
| C8 | C7 | | | | | | |
| C9 | C1 | | | | | | |
| C10 | C7 | | | | | | |
| C11 | C1 | | | | | | |
| C12 | C1 | | | | | | |
| C13 | C1 | | | | | | |
| C14 | C7 | | | | | | |
| C15 | C1 | | | | | | |
| C16 | C7 | | | | | | |
| C17 | C7 | | | | | | |
| C18 | C7 | | | | | | |
| C19 | C7 | | | | | | |
| C20 | C1 | | | | | | |
| C21 | C7 | | | | | | |
| C22 | C7 | | | | | | |
| C23 | C7 | | | | | | |
| C24 | C1 | | | | | | |
| C25 | C1 | | | | | | |
| C26 | C1 | | | | | | |
| C27 | C7 | | | | | | |
| C28 | | NOT USED | | | | | |
| C29 | C1 | | | | | | |
| C30 | C1 | | | | | | |
| C31 | C7 | | | | | | |
| C32 | C1 | | | | | | |
| C33 | C1 | | | | | | |
| C34 | C1 | | | | | | |
| C35 | C1 | | | | | | |
| C36 | C1 | | | | | | |
| C37 | C1 | | | | | | |
| C38 | C1 | | | | | | |
| C39 | C1 | | | | | | |
| C40 | C1 | | | | | | |
| C41 | C1 | | | | | | |
| C42 | C1 | | | | | | |
| C43 | C1 | | | | | | |
| C44 | | CAP,SMD,TANT | 47µF | 20% | 6V | 2100113-00 | 2 |
| C45 | C1 | | | | | | |
| C46 | C1 | | | | | | |
| C47 | C1 | | | | | | |
| C48 | C1 | | | | | | |
| C49 | C1 | | | | | | |
| C50 | | NOT USED | | | | | |
| C51 | | CAP,SMD,CER,NPO | 120PF | 5% | 50V | 2100055-00 | 1 |
| C52 | C1 | | | | | | |
| C53 | C1 | | | | | | |
| C54 | C7 | | | | | | |
| C55 | | CAP,SMD,CER,X7R | .033µF | 10% | 50V | 2100093-00 | 2 |
| C56 | C1 | | | | | | |
| C57 | C1 | | | | | | |
| C58 | C7 | | | | | | |
| C59 | C7 | | | | | | |
| C60 | C1 | | | | | | |
| C61 | C55 | | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-03 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C62 | C1 | | | | | | |
| C63 | C1 | | | | | | |
| C64 | C1 | | | | | | |
| C65 | C1 | | | | | | |
| C66 | C1 | | | | | | |
| C67 | C1 | | | | | | |
| C68 | C1 | | | | | | |
| C69 | C1 | | | | | | |
| C70 | C1 | | | | | | |
| C71 | C44 | | | | | | |
| C72 | | CAP,SMD,TANT | 10µF | 10% | 25V | 2100043-00 | 2 |
| C73 | C72 | | | | | | |
| C74 | C1 | | | | | | |
| C75 | C1 | | | | | | |
| C76 | C1 | | | | | | |
| C77 | C1 | | | | | | |
| C78 | C1 | | | | | | |
| C79 | | CAP,SMD,CER,NPO | 82PF | 5% | 50V | 2100078-00 | 1 |
| C80 | | CAP,SMD,Z5U | 1µF | 20% | 50V | 2100108-00 | 1 |
| C81 | | CAP,SMD,NPO | 3.9PF | | 50V | 2100121-00 | 1 |
| C82 | C1 | | | | | | |
| C83 | C1 | | | | | | |
| C84 | C1 | | | | | | |
| C85 | C1 | | | | | | |
| C86 | | CAP,TANTALUM | 100µF | 20% | 10V | 2300039-00 | 1 |
| C87 | C1 | | | | | | |
| C88 | | CAP,SMD,CER,NPO | 270PF | 5% | 50V | 2100079-00 | 1 |
| C89 | C1 | | | | | | |
| C90 | C1 | | | | | | |
| C91 | | CAP,ML CER | .001µF | 10% | 100V | 2150015-00 | 2 |
| C92 | C91 | | | | | | |
| CR1 | | DIODE,SMD,HSMP-3830,PIN | | | | 2700005-00 | 11 |
| CR2 | CR1 | | | | | | |
| CR3 | CR1 | | | | | | |
| CR4 | CR1 | | | | | | |
| CR5 | CR1 | | | | | | |
| CR6 | CR1 | | | | | | |
| CR7 | CR1 | | | | | | |
| CR8 | CR1 | | | | | | |
| CR9 | CR1 | | | | | | |
| CR10 | | DIODE,SMD,HSMS-2820,SCHOTTKY BARR | | | | 2740011-00 | 1 |
| CR11 | CR1 | | | | | | |
| CR12 | CR1 | | | | | | |
| CR13 | | DIODE,SMD,MMBD7000 | | | | 2740010-00 | 1 |
| CR14 | | NOT USED | | | | | |
| CR15 | | DIODE,1N914 | | | | 2700914-00 | 2 |
| CR16 | CR15 | | | | | | |
| J1 | | CONN,COAX PC RCPT,SNAP NANOHEX | | | | 2610038-00 | 7 |
| J2 | J17 | | | | | | |
| J3 | J1 | | | | | | |
| J4 | J1 | | | | | | |
| J5 | J1 | | | | | | |
| J6 | J1 | | | | | | |
| J7 | J1 | | | | | | |
| L1 | | INDUCTOR,SMD,.033µH | | | | 3530025-05 | 5 |
| L2 | | INDUCTOR,SMD,.082µH | | | | 3530025-32 | 1 |
| L3 | L1 | | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-03 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| L4 | L1 | | | | | | |
| L5 | L1 | | | | | | |
| L6 | L1 | | | | | | |
| L7 | | INDUCTOR,SMD,2.2µH | | | | 3530025-16 | 1 |
| L8 | | INDUCTOR,SMD,.100µH | | | | 3530025-08 | 1 |
| L9 | | INDUCTOR,SMD,1.5µH | | | | 3530025-15 | 1 |
| L10 | | INDUCTOR,SMD,180µH | | | | 3530024-03 | 1 |
| Q1 | | XSTR,SMD,MMBF4416,SOT-23 | | | | 4730014-00 | 1 |
| Q2 | | XSTR,MMBT3960,NPN SWITCHING | | | | 1410101-00 | 1 |
| R1 | | RES,SMD | 56.2 | 1/8W | 1% | 4235629-00 | 2 |
| R2 | | RES,SMD | 22.1 | 1/8W | 1% | 4232219-00 | 3 |
| R3 | R2 | | | | | | |
| R4 | | RES,SMD | 100 | 1/8W | 1% | 4231000-00 | 12 |
| R5 | R4 | | | | | | |
| R6 | | RES,SMD | 10.0 | 1/8W | 1% | 4231009-00 | 11 |
| R7 | | RES,SMD | 562 | 1/8W | 1% | 4235620-00 | 2 |
| R8 | | RES,SMD | 6.81K | 1/8W | 1% | 4236811-00 | 1 |
| R9 | | RES,SMD | 1K | 1/8W | 1% | 4231001-00 | 9 |
| R10 | R7 | | | | | | |
| R11 | R9 | | | | | | |
| R12 | R4 | | | | | | |
| R13 | R6 | | | | | | |
| R14 | R4 | | | | | | |
| R15 | | RES,SMD | 68.1 | 1/8W | 1% | 4236819-00 | 2 |
| R16 | R6 | | | | | | |
| R17 | R15 | | | | | | |
| R18 | | RES,SMD | 681 | 1/8W | 1% | 4236810-00 | 4 |
| R19 | | RES,SMD | 2.21K | 1/8W | 1% | 4232211-00 | 4 |
| R20 | R6 | | | | | | |
| R21 | R4 | | | | | | |
| R22 | R4 | | | | | | |
| R23 | R6 | | | | | | |
| R24 | R4 | | | | | | |
| R25 | R4 | | | | | | |
| R26 | R19 | | | | | | |
| R27 | R19 | | | | | | |
| R28 | R18 | | | | | | |
| R29 | | RES,SMD | 511 | 1/8W | 1% | 42 35110-00 | 7 |
| R30 | R2 | | | | | | |
| R31 | | RES,SMD | 110 | 1/8W | 1% | 4231100-00 | 1 |
| R32 | | RES,SMD | 82.5 | 1/8W | 1% | 4238259-00 | 1 |
| R33 | R4 | | | | | | |
| R34 | R18 | | | | | | |
| R35 | | RES,SMD | 1.10K | 1/8W | 1% | 4231101-00 | 2 |
| R36 | | RES,SMD | 825 | 1/8W | 1% | 4238250-00 | 2 |
| R37 | R1 | | | | | | |
| R38 | R4 | | | | | | |
| R39 | R6 | | | | | | |
| R40 | | RES,SMD | 221 | 1/8W | 1% | 4232210-00 | 4 |
| R41 | R6 | | | | | | |
| R42 | | RES,SMD | 301 | 1/8W | 1% | 4233010-00 | 3 |
| R43 | | RES,SMD | 10K | 1/8W | 1% | 4231002-00 | 4 |
| R44 | | NOT USED | | | | | |
| R45 | | RES,SMD | 475 | 1/8W | 1% | 4234750-00 | 4 |
| R46 | R45 | | | | | | |
| R47 | R454 | | | | | | |
| R48 | | RES,SMD | 332 | 1/8W | 1% | 4233320-00 | 7 |
| R49 | R9 | | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-03 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| R50 | R45 | | | | | | |
| R51 | R9 | | | | | | |
| R52 | R48 | | | | | | |
| R53 | R48 | | | | | | |
| R54 | R48 | | | | | | |
| R55 | R19 | | | | | | |
| R56 | R48 | | | | | | |
| R57 | | RES,SMD | 4.75K | 1/8W | 1% | 4234751-00 | 1 |
| R58 | | RES,SMD | 47.5 | 1/8W | 1% | 4234759-00 | 1 |
| R59 | R40 | | | | | | |
| R60 | R48 | | | | | | |
| R61 | R48 | | | | | | |
| R62 | R43 | | | | | | |
| R63 | | RES,SMD | 4.32K | 1/8W | 1% | 4234321-00 | 2 |
| R64 | R4 | | | | | | |
| R65 | R38 | | | | | | |
| R66 | | RES,SMD | 3.32K | 1/8W | 1% | 4233321-00 | 1 |
| R67 | R43 | | | | | | |
| R68 | | RES,SMD | 221K | 1/8W | 1% | 4232213-00 | 1 |
| R69 | R9 | | | | | | |
| R70 | R18 | | | | | | |
| R71 | R9 | | | | | | |
| R72 | | JUMPER,SMD,MINI MCR18 | | | | 5000288-00 | 6 |
| R73 | | RES,SMD | 1.82K | 1/8W | 1% | 4231821-00 | 1 |
| R74 | R36 | | | | | | |
| R75 | | RES,SMD | 365 | 1/8W | 1% | 4233650-00 | 1 |
| R76 | | RES,SMD | 182 | 1/8W | 1% | 4231820-00 | 1 |
| R77 | R43 | | | | | | |
| R78 | R9 | | | | | | |
| R79 | R9 | | | | | | |
| R80 | R72 | | | | | | |
| R81 | | RES,SMD | 2.00K | 1/8W | 1% | 4232001-00 | 1 |
| R82 | | RES,SMD | 750 | 1/8W | 1% | 4237500-00 | 1 |
| R83 | R40 | | | | | | |
| R84 | | RES,SMD | 130 | 1/8W | 1% | 4231300-00 | 1 |
| R85 | R9 | | | | | | |
| R86 | | RES,SMD | 5.11K | 1/8W | 1% | 4235111-00 | 1 |
| R87 | R4 | | | | | | |
| R88 | R42 | | | | | | |
| R89 | R42 | | | | | | |
| R90 | R72 | | | | | | |
| R91 | | RES,SMD | 100K | 1/8W | 1% | 4231003-00 | 1 |
| R92 | | RES,SMD | 1.00M | 1/8W | 1% | 4231004-00 | 1 |
| R93 | | RES,SMD | 10.0M | 1/8W | 1% | 4231005-00 | 1 |
| R94 | R6 | | | | | | |
| R95 | | RES,SMD | 1.50K | 1/8W | 1% | 4231501-00 | 1 |
| R96 | R6 | | | | | | |
| R97 | R6 | | | | | | |
| R98 | R29 | | | | | | |
| R99 | R6 | | | | | | |
| R100 | | RES,SMD | 2.74K | 1/8W | 1% | 4232741-00 | 2 |
| R101 | R29 | | | | | | |
| R102 | R29 | | | | | | |
| R103 | R29 | | | | | | |
| R104 | R72 | | | | | | |
| R105 | R100 | | | | | | |
| R106 | R29 | | | | | | |
| R107 | R40 | | | | | | |
| R108 | R63 | | | | | | |
| R109 | R29 | | | | | | |
| TP1 | | NOT USED | | | | | |
| TP2 | | NOT USED | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-03 Rev. D

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| TP3 | | NOT USED | | |
| TP4 | | NOT USED | | |
| TP5 | | NOT USED | | |
| TP6 | | NOT USED | | |
| TP7 | | NOT USED | | |
| TP8 | | NOT USED | | |
| TP9 | | NOT USED | | |
| TP10 | | NOT USED | | |
| TP11 | | NOT USED | | |
| TP12 | | NOT USED | | |
| TP13 | | NOT USED | | |
| TP14 | | NOT USED | | |
| TP15 | | NOT USED | | |
| U1 | | IC,SMD,MSA-0385,MMIC | 3170071-00 | 4 |
| U2 | U1 | | | |
| U3 | | IC,SMD,MSA-0885,AMP MMIC | 5352005-00 | 1 |
| U4 | U1 | | | |
| U5 | U1 | | | |
| U6 | | IC,SMD,10H124,TTL/MECL TRANSLATOR | 3170072-00 | 1 |
| U7 | | IC,SMD,10H104,MECL AND GATES | 3170073-00 | 1 |
| U8 | | IC,3199E,VHF/UHF,4 PRESCALER | 3043199-00 | 1 |
| U9 | | IC,AD96685,ULTRAFAST COMPARATOR | 3110126-00 | 1 |
| U10 | | IC,SMD,74HC595,8-BIT SHIFT REGISTER | 3170056-00 | 2 |
| U11 | | IC,SMD,DG403DY | 3110130-00 | 2 |
| U12 | U11 | | | |
| U13 | | IC,AD1856,16-BIT PCM AUDIO DAC | 3110129-00 | 1 |
| U14 | | IC,SMD,OP-27,OP AMP,S08 | 3170045-00 | 3 |
| U15 | U14 | | | |
| U16 | | IC,SMD,NE521 | 3170028-00 | 4 |
| U17 | U16 | | | |
| U18 | U14 | | | |
| U19 | U16 | | | |
| U20 | U16 | | | |
| U21 | | PAL,PRGM,16L8,DECODER | 2070086-00 | 1 |
| U22 | | IC,SMD,74LS279A,QUAD S-R FF | 3170080-00 | 2 |
| U23 | U22 | | | |
| U24 | | IC,SMD,74HC165,SHIFT REGISTER | 3170078-00 | 1 |
| U25 | U10 | | | |
| U26 | | IC,SMD,74S00,QUAD 2-INPUT NAND GATE | 3170079-00 | 1 |
| U27 | | IC,SMD,74HC125,QUAD 3-STATE | 3110127-00 | 1 |
| U28 | | IC,SMD,10H125,MECL/TTL TRANSLATOR | 3170070-00 | 1 |
| U29 | | IC,SMD,10216,HISP TPL LINE RCVR | 3170034-00 | 1 |
| W1 | | NOT USED | | |
| W2 | | NOT USED | | |
| W3 | R72 | | | |
| W4 | R72 | | | |
| XU1 | | NOT USED | | |
| XU2 | | NOT USED | | |
| XU3 | | NOT USED | | |
| XU4 | | NOT USED | | |
| XU5 | | NOT USED | | |
| XU6 | | NOT USED | | |
| XU7 | | NOT USED | | |
| XU8 | | CONN,SOCKET,DIP,8 PIN | 2630014-00 | 1 |
| XU9 | | NOT USED | | |
| XU10 | | NOT USED | | |
| XU11 | | NOT USED | | |
| XU12 | | NOT USED | | |
| XU13 | | NOT USED | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-03 Rev. D

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| XU14 | | NOT USED | | |
| XU15 | | NOT USED | | |
| XU16 | | NOT USED | | |
| XU17 | | NOT USED | | |
| XU18 | | NOT USED | | |
| XU19 | | NOT USED | | |
| XU20 | | NOT USED | | |
| XU21 | | CONN,SOCKET,DIP,20 PIN | 2630018-00 | 1 |
| XU22 | | NOT USED | | |
| XU23 | | NOT USED | | |
| XU24 | | NOT USED | | |
| XU25 | | NOT USED | | |
| XU26 | | NOT USED | | |
| XU27 | | NOT USED | | |
| XU28 | | NOT USED | | |
| XU29 | | NOT USED | | |
| HARDWARE USED IN THIS ASSEMBLY | | | | |
| | | HANDLE,PCB | 5230001-00 | 2 |
| | | PIN,ROLL,3/32 DIA 1/4 LG | 5110008-00 | 2 |
| | | WIRE,INSUL,18AWG GRN | 5418555-00 | 1 |
| | | PCB SCHEMATIC DIAGRAM | 5500420-03 D | REF. |

## COMPONENT COORDINATES (SIGNAL CONDITIONER ASSEMBLY A9)

| REF DES | COORD | REF DES | COORD | REF DES | COORD | REF DES | COORD | REF DES | COORD |
|---|---|---|---|---|---|---|---|---|---|
| C1 | A-1 | C59 | B-8 | L1 | A-1 | R46 | A-3 | R104 | C-12 |
| C2 | A-2 | C60 | B-8 | L2 | A-2 | R47 | A-3 | R105 | D-12 |
| C3 | A-2 | C61 | B-7 | L3 | B-1 | R48 | B-4 | R106 | D-11 |
| C4 | A-2 | C62 | B-7 | L4 | C-1 | R49 | B-4 | R107 | D-11 |
| C5 | B-1 | C63 | B-8 | L5 | D-1 | R50 | B-4 | R108 | D-12 |
| C6 | B-1 | C64 | B-2 | L6 | D-2 | R51 | C-3 | R109 | D-12 |
| C7 | B-2 | C65 | C-7 | L7 | D-2 | R52 | C-3 | | |
| C8 | B-2 | C66 | C-8 | L8 | C-3 | R53 | C-4 | TP1 | A-1 |
| C9 | C-1 | C67 | A-9 | L9 | D-2 | R54 | C-3 | TP2 | A-1 |
| C10 | C-2 | C68 | B-9 | L10 | B-7 | R55 | C-4 | TP3 | B-2 |
| C11 | C-1 | C69 | B-9 | | | R56 | C-4 | TP4 | C-2 |
| C12 | C-2 | C70 | C-9 | Q1 | B-12 | R57 | C-3 | TP5 | C-1 |
| C13 | D-1 | C71 | C-9 | Q2 | B-12 | R58 | C-3 | TP6 | D-1 |
| C14 | D-2 | C72 | C-9 | | | R59 | C-4 | TP7 | D-3 |
| C15 | B-2 | C73 | C-9 | R1 | A-2 | R60 | C-3 | TP8 | A-4 |
| C16 | C-2 | C74 | C-9 | R2 | A-2 | R61 | C-4 | TP9 | C-5 |
| C17 | D-2 | C75 | A-10 | R3 | A-2 | R62 | D-4 | TP10 | D-5 |
| C18 | A-3 | C76 | B-10 | R4 | A-1 | R63 | D-4 | TP11 | B-7 |
| C19 | B-2 | C77 | B-11 | R5 | A-1 | R64 | B-5 | TP12 | C-9 |
| C20 | B-3 | C78 | B-11 | R6 | A-1 | R65 | B-5 | TP13 | A-11 |
| C21 | C-3 | C79 | A-12 | R7 | A-1 | R66 | B-5 | TP14 | D-11 |
| C22 | C-2 | C80 | A-12 | R8 | B-1 | R67 | C-5 | TP15 | D-12 |
| C23 | C-2 | C81 | B-12 | R9 | B-1 | R68 | C-5 | | |
| C24 | C-2 | C82 | B-11 | R10 | B-1 | R69 | C-5 | U1 | A-2 |
| C25 | D-3 | C83 | B-12 | R11 | B-2 | R70 | C-5 | U2 | B-2 |
| C26 | D-3 | C84 | C-11 | R12 | B-1 | R71 | C-5 | U3 | C-2 |
| C27 | B-2 | C85 | C-12 | R13 | B-1 | R72 | A-7 | U4 | D-2 |
| C28 | D-3 | C86 | C-11 | R14 | B-1 | R73 | A-7 | U5 | C-2 |
| C29 | C-3 | C87 | C-12 | R15 | C-1 | R74 | A-8 | U6 | B-3 |
| C30 | B-3 | C88 | D-11 | R16 | C-1 | R75 | A-8 | U7 | B-3 |
| C31 | B-3 | C89 | D-12 | R17 | C-1 | R76 | A-8 | U8 | C-3 |
| C32 | C-4 | C90 | D-11 | R18 | C-2 | R77 | A-8 | U9 | D-3 |
| C33 | C-3 | C91 | B-12 | R19 | C-2 | R78 | B-7 | U10 | A-4 |
| C34 | D-3 | C92 | C-11 | R20 | C-1 | R79 | B-7 | U11 | B-4 |
| C35 | C-3 | | | R21 | C-1 | R80 | B-7 | U12 | C-4 |
| C36 | D-3 | CR1 | B-1 | R22 | C-2 | R81 | B-8 | U13 | A-5 |
| C37 | A-4 | CR2 | B-2 | R23 | D-1 | R82 | B-8 | U14 | B-5 |
| C38 | B-4 | CR3 | B-2 | R24 | D-1 | R83 | A-8 | U15 | C-5 |
| C39 | B-5 | CR4 | C-2 | R25 | D-1 | R84 | A-8 | U16 | A-7 |
| C40 | C-4 | CR5 | C-2 | R26 | B-2 | R85 | B-2 | U17 | A-8 |
| C41 | C-5 | CR6 | C-2 | R27 | B-2 | R86 | B-7 | U18 | B-2 |
| C42 | D-4 | CR7 | C-2 | R28 | C-2 | R87 | B-7 | U19 | B-8 |
| C43 | D-4 | CR8 | C-2 | R29 | C-2 | R88 | B-8 | U20 | B-8 |
| C44 | D-5 | CR9 | C-2 | R30 | D-2 | R89 | B-8 | U21 | C-7 |
| C45 | A-5 | CR10 | D-2 | R31 | D-2 | R90 | A-11 | U22 | A-9 |
| C46 | B-5 | CR11 | B-2 | R32 | A-3 | R91 | A-12 | U23 | B-9 |
| C47 | B-5 | CR12 | B-2 | R33 | B-3 | R92 | A-12 | U24 | C-9 |
| C48 | B-5 | CR13 | C-4 | R34 | B-3 | R93 | B-11 | U25 | A-10 |
| C49 | B-6 | CR15 | A-12 | R35 | B-3 | R94 | B-11 | U26 | B-10 |
| C50 | C-5 | CR16 | A-12 | R36 | B-2 | R95 | B-12 | U27 | C-10 |
| C51 | C-5 | | | R37 | C-3 | R96 | B-12 | U28 | A-11 |
| C52 | C-5 | J1 | A-2 | R39 | C-3 | R97 | B-11 | U29 | D-11 |
| C53 | C-5 | J2 | B-2 | R40 | C-2 | R98 | B-12 | | |
| C54 | A-7 | J3 | A-3 | R41 | B-3 | R99 | B-12 | W3 | C-10 |
| C55 | A-7 | J4 | B-3 | R42 | D-2 | R100 | C-12 | W4 | C-10 |
| C56 | A-9 | J5 | A-4 | R43 | D-3 | R101 | C-11 | | |
| C57 | A-8 | J6 | A-7 | R44 | D-3 | R102 | C-11 | XU8 | C-3 |
| C58 | B-7 | J7 | A-11 | R45 | A-3 | R103 | C-12 | XU21 | C-7 |

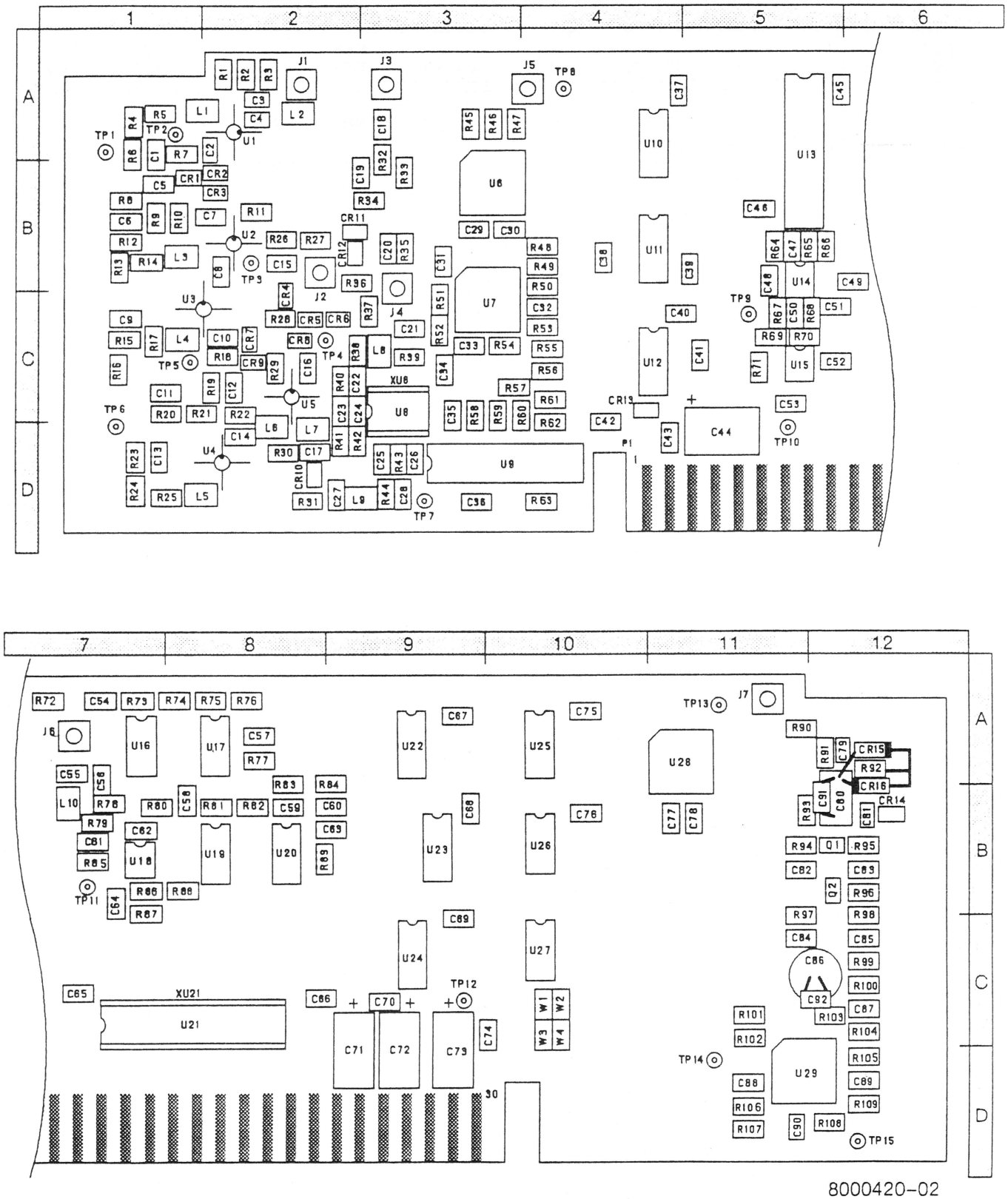


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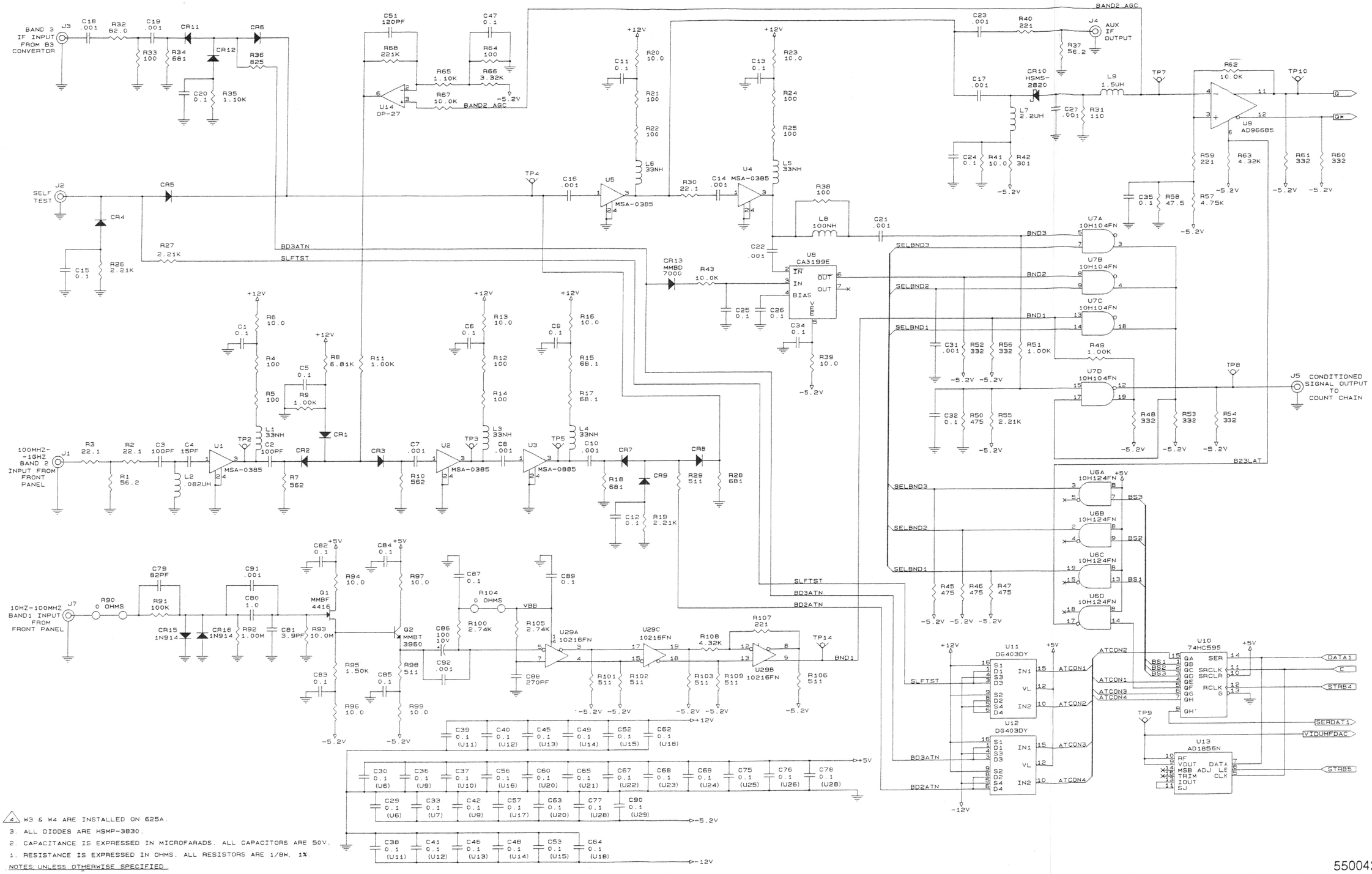
Figure 10-25. Signal Conditioner (A9) Component Locator.




⚠4 W3 & W4 ARE INSTALLED ON 625A.

3. ALL DIODES ARE HSMP-3830.

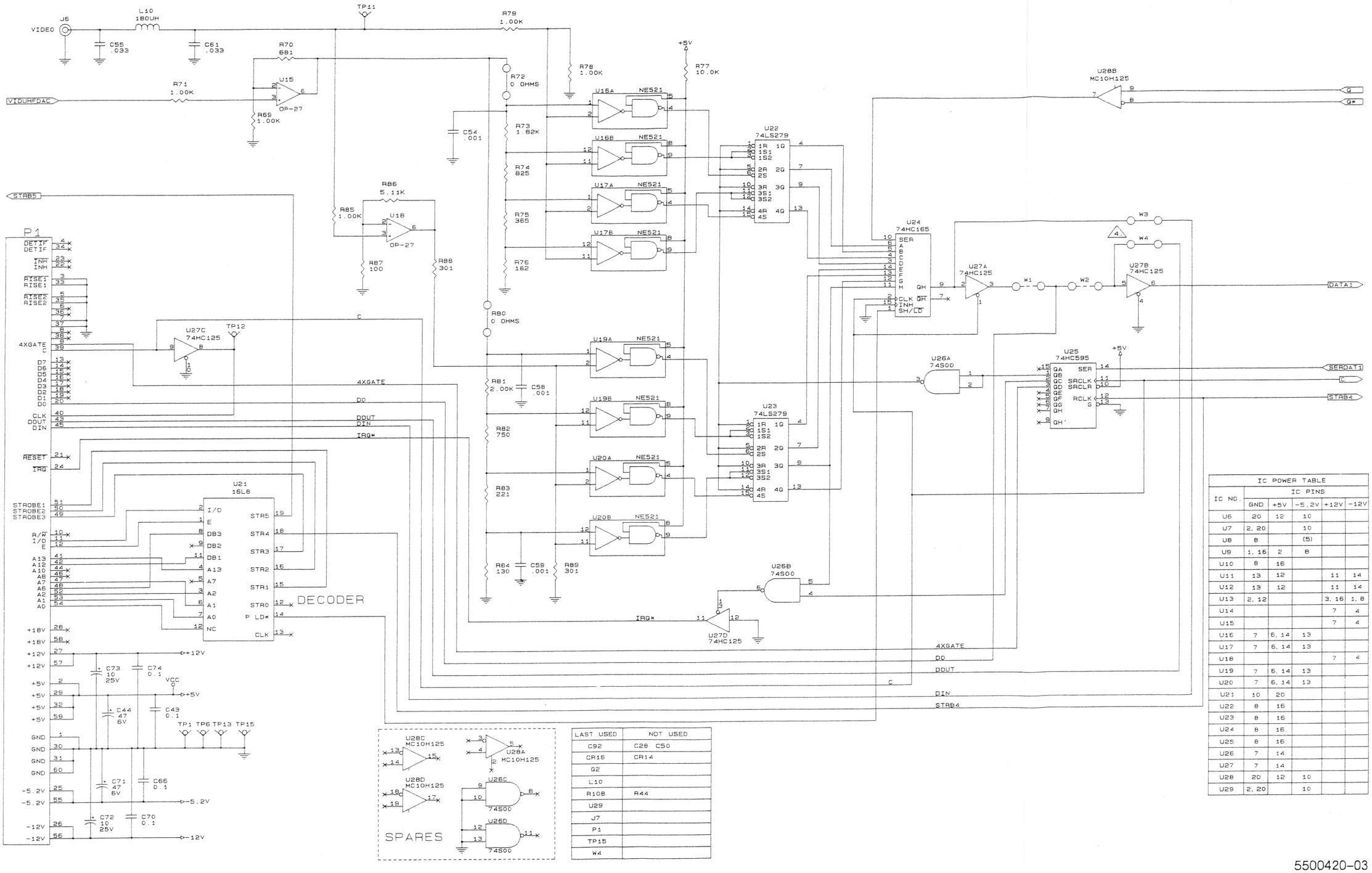
2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W, 1%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500420-03

Figure 10-26. Signal Conditioner (
Schematic Diagram.
(Sheet 1 of 2)




| IC POWER TABLE | | | | | |
|---|---|---|---|---|---|
| IC NO. | IC PINS | | | | |
| | GND | +5V | -5.2V | +12V | -12V |
| U6 | 20 | 12 | 10 | | |
| U7 | 2, 20 | | 10 | | |
| U8 | 8 | | (5) | | |
| U9 | 1, 16 | 2 | 8 | | |
| U10 | 8 | 16 | | | |
| U11 | 13 | 12 | | 11 | 14 |
| U12 | 13 | 12 | | 11 | 14 |
| U13 | 2, 12 | | | 3, 16 | 1, 8 |
| U14 | | | | 7 | 4 |
| U15 | | | | 7 | 4 |
| U16 | 7 | 5, 14 | 13 | | |
| U17 | 7 | 5, 14 | 13 | | |
| U18 | | | | 7 | 4 |
| U19 | 7 | 5, 14 | 13 | | |
| U20 | 7 | 5, 14 | 13 | | |
| U21 | 10 | 20 | | | |
| U22 | 8 | 16 | | | |
| U23 | 8 | 16 | | | |
| U24 | 8 | 16 | | | |
| U25 | 8 | 16 | | | |
| U26 | 7 | 14 | | | |
| U27 | 7 | 14 | | | |
| U28 | 20 | 12 | 10 | | |
| U29 | 2, 20 | | 10 | | |

| LAST USED | NOT USED |
|---|---|
| C92 | C28 C50 |
| CR15 | CR14 |
| G2 | |
| L10 | |
| R108 | R44 |
| U29 | |
| J7 | |
| P1 | |
| TP15 | |
| W4 | |

5500420-03 D

Figure 10-26. Signal Conditioner (A
Schematic Diagram.
(Sheet 2 of 2)

# A10
# BAND 3 MICROWAVE CONVERTER
# (2010864-01)

**NOTE**

Due to the extensive test equipment and special processes required to test and repair this assembly, field repair of this assembly is not recommended. For this reason the information contained in this section is limited to what is necessary for troubleshooting to the assembly level. Exchange modules are available from EIP. Please consult the factory for pricing.

## CAUTION

**Attempted disassembly or repair of the microwave converter will void warranty and prevent the unit from being accepted for module exchange or repair.**

The Band 3 Microwave Converter is a complete microwave downconverter consisting of five subassemblies: YIG, VCO, AFC, IF, and YIG driver.

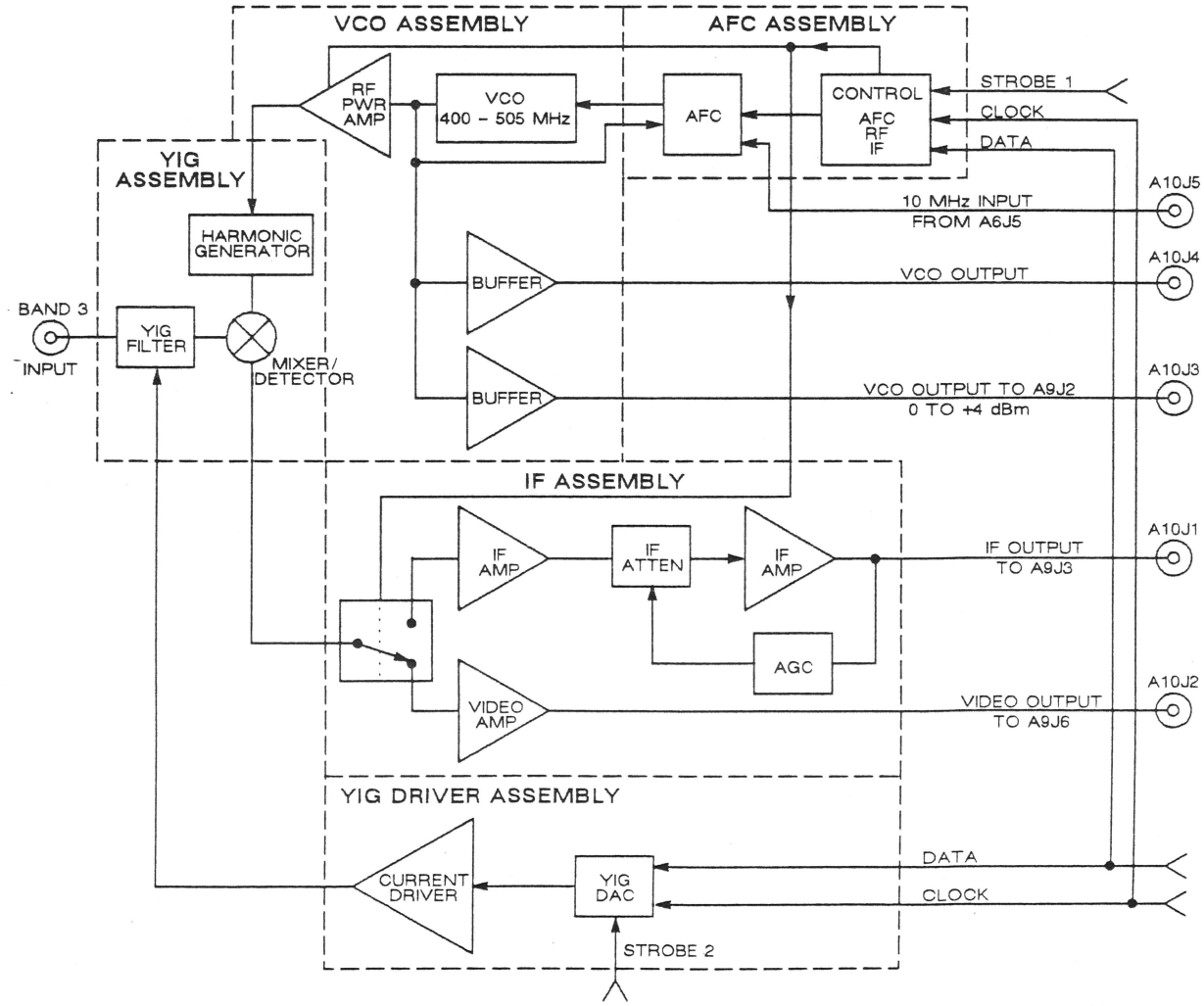



Figure 10-27. Band 3 Microwave Converter Functional Block Diagram.

The YIG assembly consists of the YIG filter, harmonic generator, and mixer. The YIG filter is an electronically tunable, narrow bandpass microwave filter having a bandpass of approximately 25 MHz and a rolloff of approximately 12 dB per octave. The filter eliminates all but the desired signal from reaching the input mixer. The harmonic generator receives its input from the synthesized VCO signal and generates harmonics of the VCO signal. One of these harmonics mixes with the incoming signal to produce the IF signal.

The VCO assembly contains a 400 to 505 MHz voltage controlled oscillator, a power amplifier, and two buffer amplifiers. The power amplifier boosts the VCO output power to approximately +28 dBm and is used to drive the harmonic generator.

The AFC assembly consists of AFC and VCO frequency control circuitry. The AFC assembly, along with the VCO, form a programmable phase lock loop that allows the VCO frequency to be precisely set, in 100 kHz increments, from 400 to 505 MHz.

The IF assembly contains a video amplifier, two IF amplifiers, and a variable IF attenuator. This assembly allows the IF signal level to be adjusted to the optimum level for counting and amplifying the video signal.

The YIG driver allows microprocessor control of troubleshooting and isolating of the YIG filter, IF attenuator, and millimeter wave IF attenuator. Technical information on the YIG driver is presented in this section to aid in distinguishing between problems in the main counter and problems in the Band 3 Microwave Converter.

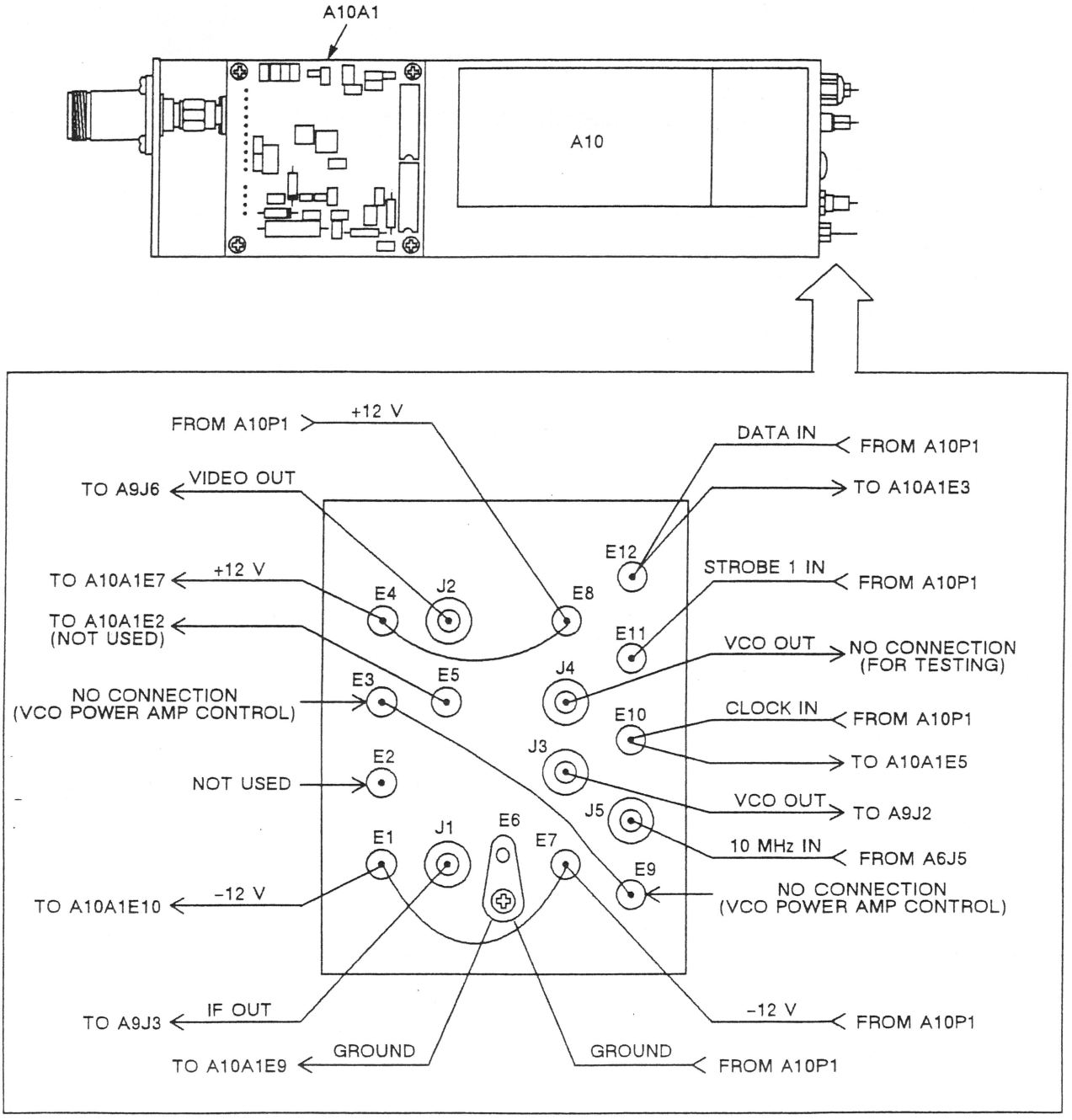
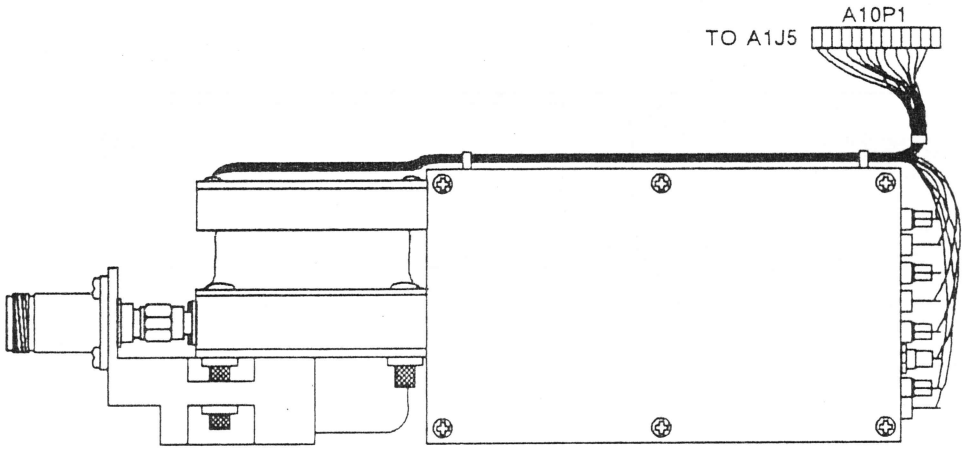



Figure 10-28. Band 3 Microwave Converter.




| A1J5 | A10P1 | | |
|---|---|---|---|
| 1 | 1 | GND → | A10E6 and A10A1E9 |
| 2 | 2 | NO CONNECTION ← | A10A1E1 |
| 3 | 3 | KEY | |
| 4 | 4 | DATA → | A10E12 and A10A1E3 |
| 5 | 5 | CLK → | A10A1E5 and A10E10 |
| 6 | 6 | +18 V → | A10A1E11 |
| 7 | 7 | +12 V → | A10A1E7, A10E8, and A10E4 |
| 8 | 8 | STR 1 → | A10E11 |
| 9 | 9 | -12 V → | A10E7, A10E1, and A10A1E10 |
| 10 | 10 | GND → | A10A1E8 |
| 11 | 11 | STR 2 → | A10A1E6 |
| 12 | 12 | STR 3 → | A10A1E4 |
| 13 | 13 | X | |

Figure 10-29. Band 3 Microwave Converter Interconnections.

## A10A1
## YIG DRIVER
## (2020390-08)

The YIG driver serves two major functions:

1. Converts serial data from the microprocessor into the current drive required to tune the YIG filter.

2. Converts serial data from the microprocessor into the voltage required to adjust the Band 3 IF attenuator.

When tuning the YIG filter, serial data from the D0 line of the microprocessor data bus is applied to the YIG DAC (U2) at pin 7. An active high latch enable signal on U2 pin 6 causes the data to be read into the DAC. The DAC converts the data into an analog output voltage which is applied to U4, a voltage-to-current converter. The signal is then amplified by Q2 to the level required to drive the YIG filter.

When adjustment of the Band 3 IF attenuator is necessary, serial data from the D0 line of the microprocessor data bus is applied to the attenuator DAC (U1) at pin 7. An active high latch enable signal on U1 pin 6 causes the data to be read into the DAC. The DAC converts the data into an analog output voltage. For Band 3 operation, the signal is used directly to control the Band 3 IF attenuator.

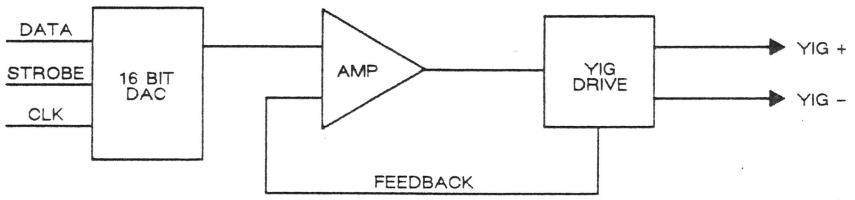



**Figure 10-30. YIG Driver Functional Block Diagram.**

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## A10A1 YIG DRIVER 2020390-08 Rev. C

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,SMD,Z5U | .1µF | 20% | 50V | 2100046-00 | 4 |
| C2 | | CAP,SMD,CER,X7R | .015µF | 10% | 50V | 2100089-00 | 1 |
| C3 | | NOT USED | | | | | |
| C4 | | NOT USED | | | | | |
| C5 | C1 | | | | | | |
| C6 | | CAP,SMD,Z5U | 1µF | 20% | 50V | 2100108-00 | 1 |
| C7 | | CAP,SMD,CER,NPO | 470PF | 5% | 50V | 2100033-00 | 1 |
| C8 | C1 | | | | | | |
| C9 | C1 | | | | | | |
| CR1 | | DIODE,SMD,MMBD7000 | | | | 2740010-00 | 1 |
| CR2 | | DIODE,1N4757,ZENER 51V | | | | 2704757-00 | 1 |
| CR3 | | DIODE,1N4003,GP RECTIFIER | | | | 2700004-00 | 1 |
| Q1 | | XSTR,SMD,TIP127 | | | | 4730010-00 | 1 |
| Q2 | | XSTR,SMD,MMBT4124,SOT-23 | | | | 4730012-00 | 1 |
| R1 | | NOT USED | | | | | |
| R2 | | NOT USED | | | | | |
| R3 | | NOT USED | | | | | |
| R4 | | RES,M/OX | 8.25K | 1/8W | 1% | 4010917-00 | 1 |
| R5 | | NOT USED | | | | | |
| R6 | | NOT USED | | | | | |
| R7 | | RES,SMD | 1% | 1/8W | 1.00K | 4231001-00 | 3 |
| R8 | R7 | | | | | | |
| R9 | R7 | | | | | | |
| R10 | | RES,SMD | 1% | 1/8W | 10.0K | 4231002-00 | 1 |
| R11 | | RES,WW | 5 OHMS | 3W | 1% | 4110027-00 | 1 |
| U1 | | NOT USED | | | | | |
| U2 | | IC,AD1856,16-BIT PCM AUDIO DAC | | | | 3110129-00 | 1 |
| U3 | | NOT USED | | | | | |
| U4 | | IC,SMD,OP-27,OP AMPL,S08 | | | | 3170045-00 | 1 |
| | | PCB SCHEMATIC DIAGRAM | | | | 5500390-08 B | REF. |

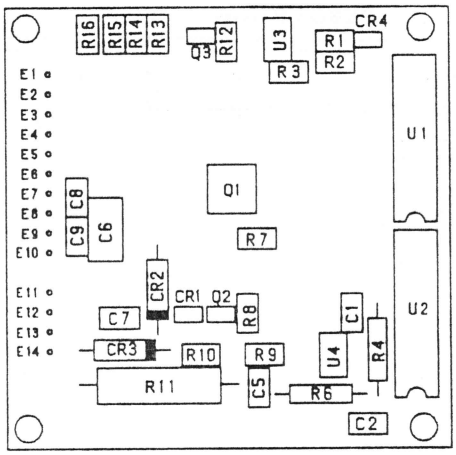
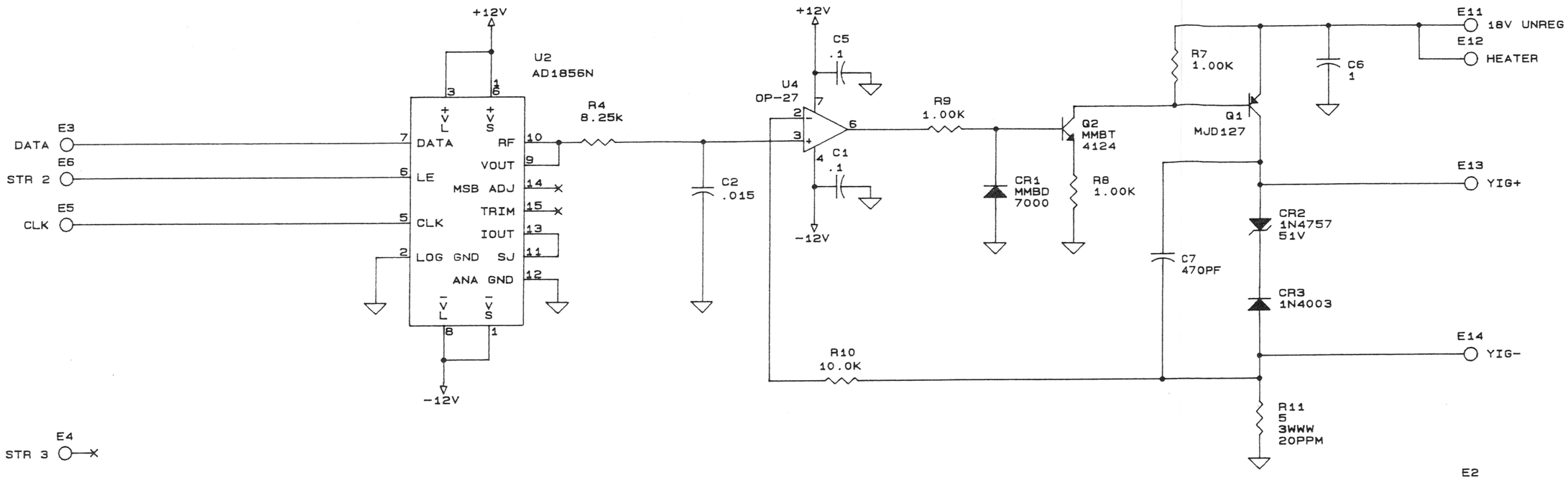



Figure 10-31. YIG Driver (A10A1) Component Locator.




| LAST USED | NOT USED |
|---|---|
| C9 | C3, C4 |
| R11 | R1, R2, R5, R6 |
| CR3 | |
| Q3 | |
| U4 | U3 |
| E14 | |

2. CAPACITANCE IS EXPRESSED IN MICROFARADS.
   ALL CAPACITORS ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W, 1%.

5500390-08

Figure 10-32. YIG Driver (A10A1) Schematic Diagra

# A12
# FRONT PANEL
# 2010829-02

The Front Panel assembly consists of the metal panel, front panel overlay, keyboard, power switch, signal input connectors, and two printed circuit boards: A12A1 and A12A2.

The Front Panel Display/Keyboard assembly (A2A1) consists of 12 numeric displays, 13 status indicators, and 18 keyboard switches.

The Front Panel Display Driver/Logic assembly (A12A2) contains the digit drivers, segment drivers, and other electronic circuitry required to provide the electronic interface between the microprocessor and the display. All information between the microprocessor and the display assembly is routed from the Motherboard at A1J1, via a 26 pin ribbon cable, to connector P1 on A12A2, the Front Panel Display Driver/Logic assembly. Figure 10-34 is a functional block diagram of the printed circuit boards for the front panel .

To prevent digital noise created in the display from interfering with instrument performance, a separate 5 volt regulator is used for the Front Panel assembly. This regulator is mounted on the Motherboard (A1) near the center of the front panel, and is connected to the front panel at A12A2P1.

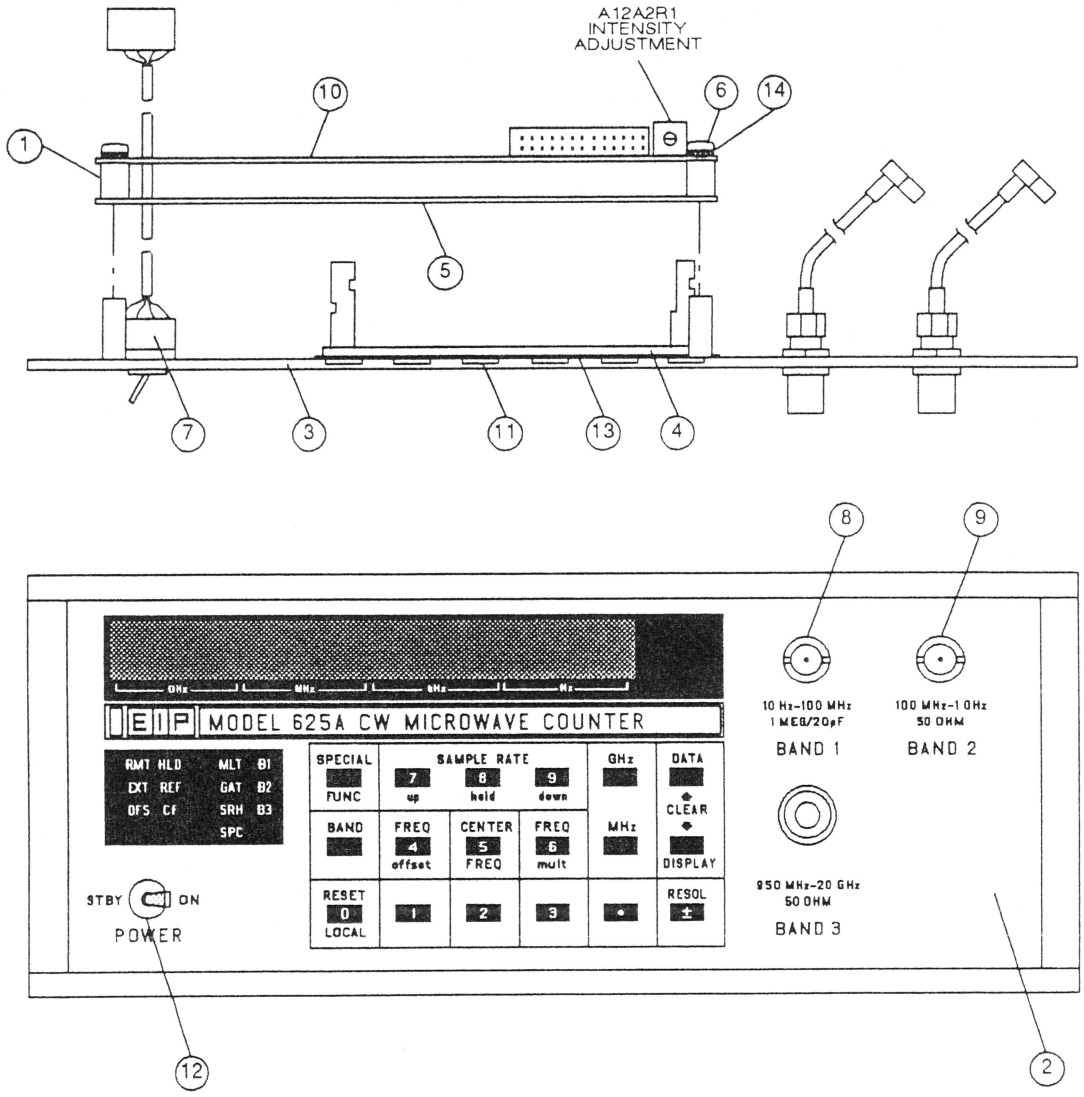



Figure 10-33. Front Panel (A12).

## A12 FRONT PANEL 2010829-02 Rev. C

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | SPACER,RND,#6,.25 ODX.140 IDX.20 LG | 5210868-02 | 2 |
| 2 | OVERLAY,FRONT PANEL,625A | 5210841-01 | 1 |
| 3 | PANEL,FRONT | 5210846-02 | 1 |
| 4 | KEY,RETAINER | 5000359-00 | 1 |
| 5 | PCB ASSY,FR PNL DSPL/KYBD,A12A1 | 2020415-01 | 1 |
| 6 | SCR,PNH X-REC SLFLKG 6-32X9/16 UNC | 5124006-09 | 2 |
| 7 | SWITCH ASSY,POWER | 2010841-01 | 1 |
| 8 | CABLE ASSY,COAX,BAND 1 INPUT | 2040487-01 | 1 |
| 9 | CABLE ASSY,COAX,BAND 2 INPUT | 2040293-01 | 1 |
| 10 | PCB ASSY,DSPL DRIVER/LOGIC,A12A2 | 2020419-01 | 1 |
| 11 | BUTTON,SET GRAY | 5210844-00 | 1 |
| 12 | DRESSNUT,CAPTIVATING | 5000357-00 | 1 |
| 13 | TAPE,MASKING,ADHESIVE 2 SIDES | 5601003-00 | 3 IN |
| 14 | WASHER,FIBRE,NO. 6 | 5000064-00 | 2 |

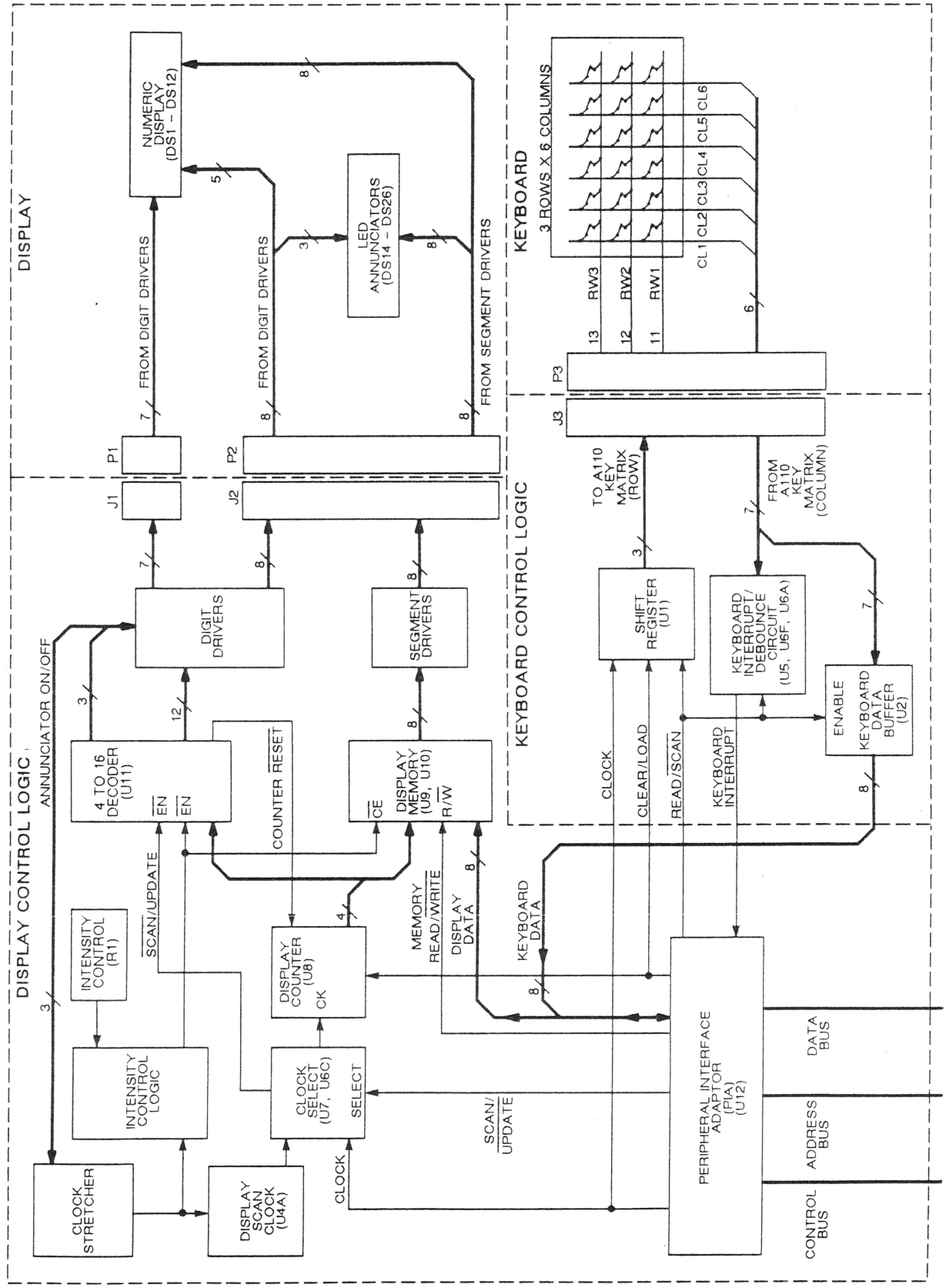



Figure 10-34. Front Panel Functional Block Diagram.

# A12A1
# FRONT PANEL DISPLAY/KEYBOARD
# (2020415-01)

The Front Panel Display/Keyboard assembly is divided into two functional sections:

- Numeric display and annunciators
- Keyboard

## NUMERIC DISPLAY AND ANNUNCIATORS

The numeric display and status annunciators are a time multiplexed display consisting of 12 common-anode 7-segment numeric display units (DS1-DS12), and 13 red annunciator LEDs (DS14-DS26) arranged in three groups. The cathode segments of each numeric display and each LED in the three groups of annunciators are connected to a common 8-line segment bus which is driven by the segment drivers on the Front Panel Display Driver/Logic assembly (A12A2). The common anodes of each numeric display and each group of annunciators are connected, through separate lines, to one to the 15 digit drivers located on the Front Panel Display Driver/Logic assembly (A12A2). The digit drivers provide the control signals that enable the numeric displays and annunciator LEDs.

## KEYBOARD

This keyboard consists of 18 single-pole, double-throw switches arranged in a 3-row by 6-column matrix.

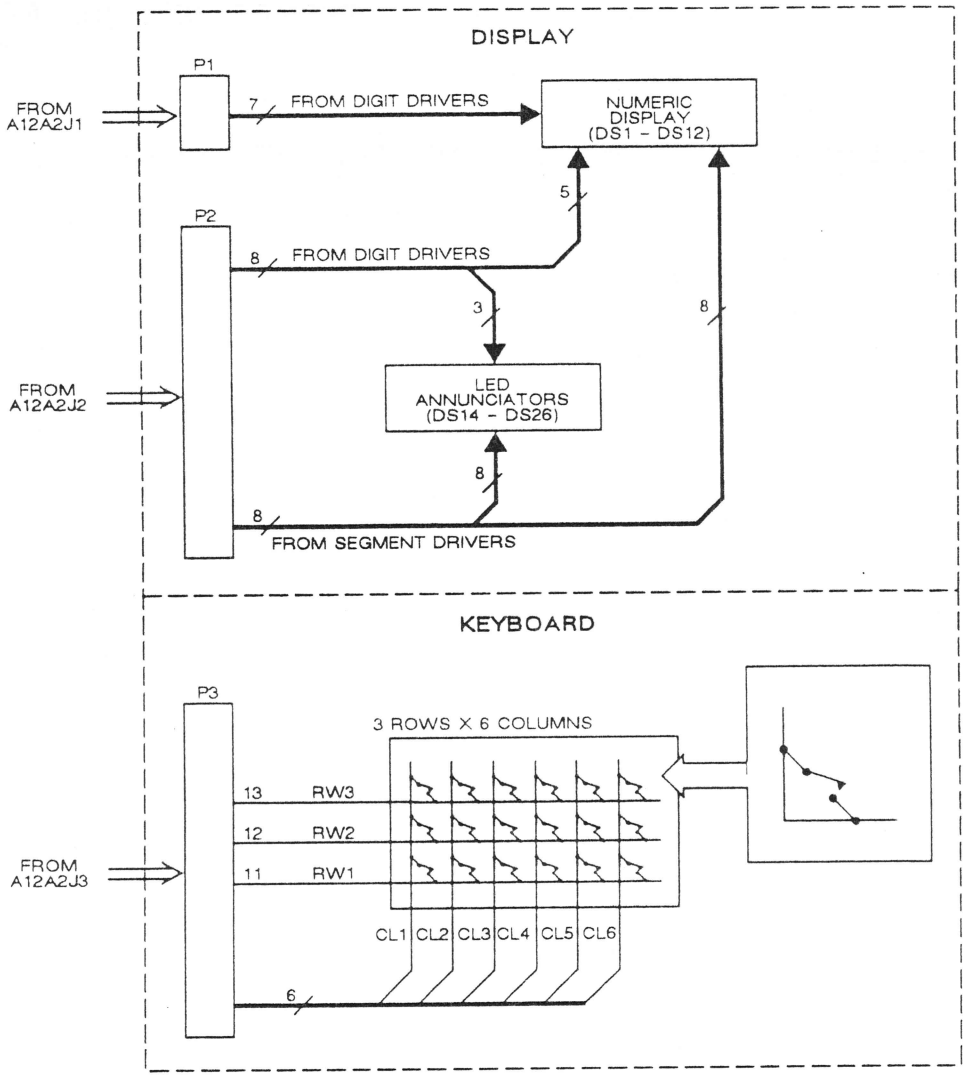



Figure 10-35. Front Panel Display/Keyboard Functional Block Diagram.

## A12A1 FRONT PANEL DISPLAY/KEYBOARD 2020415-01 Rev. E

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| DS1 | | 7-SEG DISPLAY,RED,COM ANODE | 2800036-00 | 12 |
| DS2 | DS1 | | | |
| DS3 | DS1 | | | |
| DS4 | DS1 | | | |
| DS5 | DS1 | | | |
| DS6 | DS1 | | | |
| DS7 | DS1 | | | |
| DS8 | DS1 | | | |
| DS9 | DS1 | | | |
| DS10 | DS1 | | | |
| DS11 | DS1 | | | |
| DS12 | DS1 | | | |
| DS13 | | NOT USED | | |
| DS14 | | LAMP,LED LIGHT BAR,RED | 2800034-00 | 13 |
| DS15 | DS14 | | | |
| DS16 | DS14 | | | |
| DS17 | DS14 | | | |
| DS18 | DS14 | | | |
| DS19 | DS14 | | | |
| DS20 | DS14 | | | |
| DS21 | DS14 | | | |
| DS22 | DS14 | | | |
| DS23 | DS14 | | | |
| DS24 | DS14 | | | |
| DS25 | DS14 | | | |
| DS26 | DS14 | | | |
| DS27 | | NOT USED | | |
| DS28 | | NOT USED | | |
| DS29 | | NOT USED | | |
| DS30 | | NOT USED | | |
| DS31 | | NOT USED | | |
| DS32 | | NOT USED | | |
| DS33 | | NOT USED | | |
| DS34 | | NOT USED | | |
| DS35 | | NOT USED | | |
| DS36 | | NOT USED | | |
| P1 | | CONN,PCB RCPT,9 PIN | 2620065-00 | 1 |
| P2 | | CONN,PCB RCPT,17 PIN | 2620067-00 | 1 |
| P3 | | CONN,PCB RCPT,13 PIN | 2620066-00 | 1 |
| S1 | | SWITCH,MOM SPDT | 4500013-00 | 18 |
| S2 | S1 | | | |
| S3 | S1 | | | |
| S4 | S1 | | | |
| S5 | S1 | | | |
| S6 | S1 | | | |
| S7 | S1 | | | |
| S8 | S1 | | | |
| S9 | S1 | | | |
| S10 | S1 | | | |
| S11 | S1 | | | |
| S12 | S1 | | | |
| S13 | S1 | | | |
| S14 | S1 | | | |
| S15 | S1 | | | |
| S16 | S1 | | | |
| S17 | S1 | | | |
| S18 | S1 | | | |
| XDS2A | | SOCKET,SIP,5 POS,LOW PRO | 2620282-00 | 24 |
| XDS2B | XDS2A | | | |

## A12A1 FRONT PANEL DISPLAY/KEYBOARD (Continued) 2020415-01 Rev. E

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| XDS3A | XDS2A | | | |
| XDS3B | XDS2A | | | |
| XDS4A | XDS2A | | | |
| XDS4B | XDS2A | | | |
| XDS5A | XDS2A | | | |
| XDS5B | XDS2A | | | |
| XDS6A | XDS2A | | | |
| XDS6B | XDS2A | | | |
| XDS7A | XDS2A | | | |
| XDS7B | XDS2A | | | |
| XDS8A | XDS2A | | | |
| XDS8B | XDS2A | | | |
| XDS9A | XDS2A | | | |
| XDS9B | XDS2A | | | |
| XDS10A | XDS2A | | | |
| XDS10B | XDS2A | | | |
| XDS11A | XDS2A | | | |
| XDS11B | XDS2A | | | |
| XDS12A | XDS2A | | | |
| XDS12B | XDS2A | | | |
| XDS13 | | NOT USED | | |
| XDS14 | | CONN,IC PIN (MINISERT)<br>SEE NOTE 1 | 2620054-00 | 26 |
| XDS15 | XDS14 | | | |
| XDS16 | XDS14 | | | |
| XDS17 | XDS14 | | | |
| XDS18 | XDS14 | | | |
| XDS19 | XDS14 | | | |
| XDS20 | XDS14 | | | |
| XDS21 | XDS14 | | | |
| XDS22 | XDS14 | | | |
| XDS23 | XDS14 | | | |
| XDS24 | XDS14 | | | |
| XDS25 | XDS14 | | | |
| XDS26 | XDS14 | | | |
| XDS26 | | NOT USED | | |
| XDS27 | | NOT USED | | |
| XDS28 | | NOT USED | | |
| XDS29 | | NOT USED | | |
| XDS30 | | NOT USED | | |
| XDS31 | | NOT USED | | |
| XDS32 | | NOT USED | | |
| XDS33 | | NOT USED | | |
| XDS34 | | NOT USED | | |
| XDS35 | | NOT USED | | |
| XDS36 | | NOT USED | | |
| | | PCB SCHEMATIC DIAGRAM | 5500415-01 B | REF. |

NOTE 1: EACH XDS-NN REF. DES. REQUIRES 2 MINISERTS.

## Front Panel Display/Keyboard Component Locator (PCB Assembly A12A1)

(See following page)

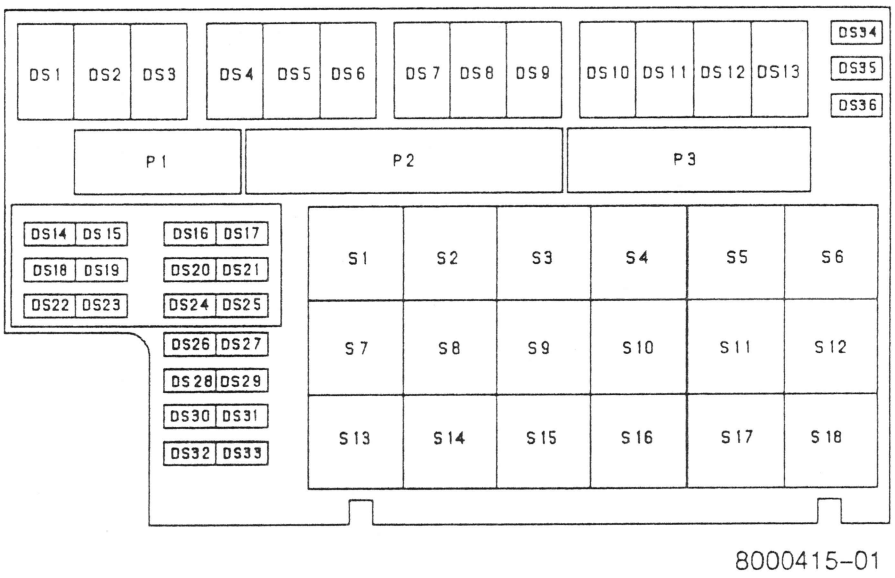
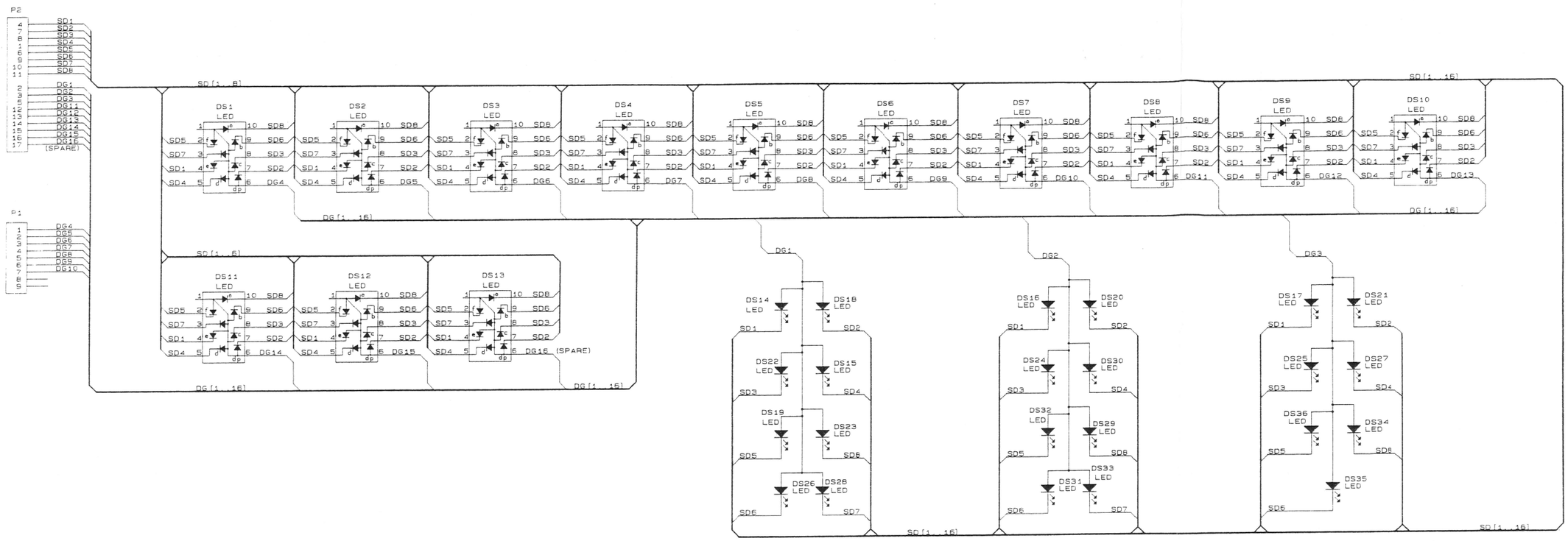
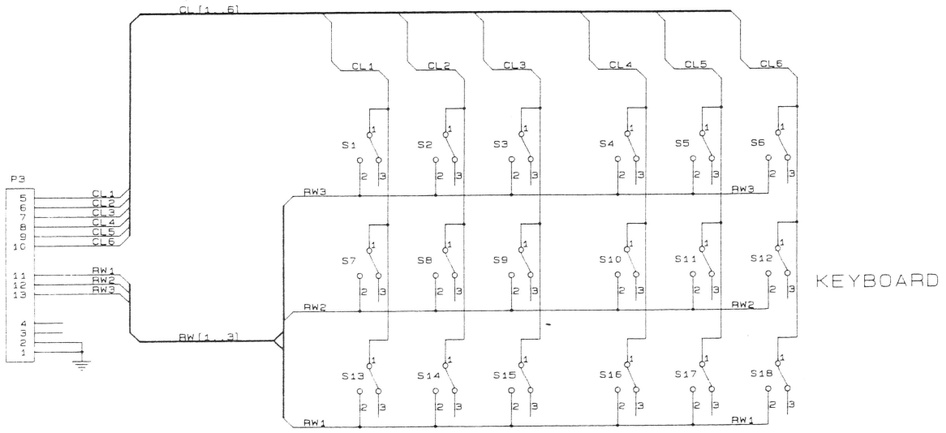



Figure 10-36. Front Panel Display/Keyboard (A12A1) Component Locator.




KEYBOARD

NOTES: UNLESS OTHERWISE SPECIFIED.

| LAST USED | NOT USED |
|---|---|
| DS36 | ---- |
| P3 | ---- |
| S18 | ---- |
| | ---- |
| | ---- |
| | ---- |

5500415-01

Figure 10-37. Front Panel Display/Keyboard (A12 Schematic Diagram.

# A12A2
# FRONT PANEL DISPLAY DRIVER/LOGIC
# (2020419-01)

The Front Panel Display Driver/Logic assembly contains the circuitry for two primary functions:

- Display control
- Keyboard control

## DISPLAY CONTROL

The signals that drive the front panel display are provided by the display memory and the multiplexing circuitry contained on the Front Panel Display Driver/Logic assembly. Display control consists of two modes of operation: the display scan mode, and the memory update mode. In the display scan mode, the data contained in the display memory is sequentially written to each of the 12 numeric displays and three groups of annunciator LEDs. In the memory update mode, the front panel display is disabled, and new data is written into the display memory by the microprocessor.

### DISPLAY SCAN MODE

In the display scan mode, the scan clock, from U4A, clocks the display counter, U8. The binary output of the display counter is applied to both the display memory and to the 4-to-16 line decoder, U11. The output from the decoder is applied to the digit drivers that sequentially enable the front panel displays and annunciator LEDs. As a particular numeric display or group of annunciators is enabled, the display memory outputs the corresponding data, lighting the appropriate display segments and annunciators.

The scan clock signal is generated by U4A, U3D and U6D. U4A is normally a monostable multivibrator, but U3D and U6D provide the delay and feedback necessary to retrigger U4A, which enables U4A to generate the scan clock. The display scan clock from U6D pin 8 is applied to the clock select circuit at U7 pin 10. Based on the inputs to U7 at pins 9 and 13, U7 will either pass the scan clock at U7 pin 10 or the clock from the microprocessor at U7 pin 12. During display scan, U7 pin 9 is high and U7 pin 13 is low, causing the display scan clock to pass through U7 to U8 pin 2, the display counter. The display counter is a 4-bit binary counter. The binary output from U8 is directed to both U11, a 4-to-16 line decoder, and to the address lines of the display memory. As the binary counter advances through its count, each of the outputs from U11 successively goes low. The low outputs from U11 are applied to the 15 digit drivers. A low output from U11 turns on a digit driver, enabling a particular numeric display or group of annunciator LEDs on the front panel. When U11 pin 16 goes low, the low signal is applied to U8 pin 9, resetting the binary counter to zero.

The binary data from display counter U8 is also applied to the address lines of the display memory U9 and U10. As the display counter advances through its count, the display memory outputs data corresponding to the enabled numeric display or group of annunciator LEDs. The segment data is then applied to the segment drivers, prior to being applied to the segment bus on the display board. The combination of a digit enable signal and segment data causes each numeric display or group of annunciator LEDs to display the proper information.

The intensity of the display is adjusted by changing the length of time that each display is enabled. During each clock cycle, decoder U11 is disabled for a period of time by the TTL high signal applied from U4B to U11 pin 18. Adjusting potentiometer R1 changes the RC time constant of U4B, which controls the amount of time each display is enabled. Decreasing the resistance of R1 increases the length of time that each display is enabled, which increases the intensity of the display.

### MEMORY UPDATE MODE

The memory update mode alternates with the display scan mode in the display control cycle. In the memory update mode, the front panel display is disabled while the display memory is updated with new display information from the microprocessor.

To update the display memory, the microprocessor first sets the display scan/$\overline{\text{update}}$ line from PIA U12 pin 6 to a logic "0." This applies a TTL high signal through inverter U6C to U7 pin 13, and a TTL low at U7 pin 9, causing U7 to pass the microprocessor-controlled clock at U7 pin 12 through U7 to U8 pin 2, the clock input for the display counter. The high TTL signal from inverter U6C is also directed to pin 19 of decoder U11, causing the output from U11 to remain high, which disables the front panel display during memory update. The clear/load line from U12 pin 7 is then set to a TTL high by the microprocessor and applied to NAND gate U3C at pin 10. The other input to the NAND gate comes from the scan/$\overline{\text{update}}$ line through inverter U6C. Since this line is also high, the output from U3C at pin 8 is low. This low is applied to display counter U8 pin 1, clearing the counter. The low on the display scan/$\overline{\text{update}}$ line is also applied to U4B at pin 11, which clears U4B causing the output at U4B pin 5 to go low. This low is applied to the display memory U9 and U10 pin 2, which enables the display memory. The microprocessor then provides display data at U12 pins 10 through 17. The read/$\overline{\text{write}}$ line from PIA U12 pin 8 is cycled high-low-high causing the data to be stored into the display memory at the addressed location. The display counter is then clocked by the microprocessor, incrementing the display counter to the next memory address. This process is rejected until all 15 bytes of display data are stored in display memory.

After all the display data is written to the display memory in the memory update mode, the display control is returned to the scan mode. This process begins with the microprocessor setting the display scan/$\overline{\text{update}}$ line high which allows the scan clock to pass through U7 to the display counter U8. The high on the display scan/$\overline{\text{update}}$ line is inverted by U6C and applied as a low at U11 pin 19, enabling decoder U11 and, effectively, the front panel display. At this point the microprocessor controlled memory read/$\overline{\text{write}}$ line from PIA U12 pin 8 is high which allows the display memory to output the stored data as addressed by the display counter.

## KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the keyboard read/$\overline{\text{scan}}$ line from U12 pin 2 is low. This low is inverted by U6E and applied to pins 1 and 19 of data buffer U2, disabling the outputs from U2. The low is also applied, as a clear, to shift register U1 pin 1, causing all the outputs from U1 (pins 12 through 15) to be low.

In the keyboard scan mode all the inputs to NAND gate U5 are normally high due to the pullup resistors contained in RN1. When a key is pressed, the row and column corresponding to that key are connected together. Since the rows are all connected to the low outputs of U1, the column corresponding to the key pressed will go low. The low is connected to U5 which causes the output of U5 to go high. This high is applied to inverter U6F in the key debounce circuit, driving the output of U6F low. The low at U6F pin 12 forward-biases diode CR1, causing capacitor C4 to begin discharging. When the voltage across C4 drops to approximately 0.7 V, the output from U6A will go high. The high output from U6A pin 2 causes a keyboard interrupt to be generated, indicating that a key is being pressed.

### READ KEYBOARD

When a key is pressed, a keyboard interrupt is sent to the microprocessor. The microprocessor responds by reading the keyboard to determine the coordinates of the key pressed.

The microprocessor begins the keyboard read sequence by placing a high on the read/$\overline{\text{scan}}$ line at U12 pin 2. This high is inverted to a low by U6E and applied to data buffer U2 pin 19, enabling it to output data. The high from U12 pin 2 is also applied to the active low clear input of U1 at pin 1. Next, the microprocessor puts a high on U12 pin 7, the clear/load line. Both the clear/load line and the read/$\overline{\text{scan}}$ line are applied to U3B pins 4 and 5, causing the output from U3B pin 6 to go low. The low at U3B pin 6 is applied to the shift/load input of shift register U1. The data at the parallel inputs of U1, a binary 1110, is then loaded into the shift register, and the low on the LSB output of U1 is applied to a row of the keyboard. The microprocessor then reads the 8 bit binary word corresponding to that row from the parallel outputs of data buffer U2. If the data read from the data buffer has a value of FF, then no key in that particular row is pressed, and the shift register is clocked again. A low is then applied to the next keyboard row and the data buffer output read by the microprocessor. This process is repeated until the output of data buffer U2 yields a value other than FF, indicating a key pressed in the corresponding row. At this time, the coordinates of the key pressed are determined by the microprocessor. The row number is determined by the number of times that the shift register was shifted; the column number is determined by the value of the 8-bit binary word read at the parallel output of data buffer U2.

After the keyboard read routine is completed the microprocessor puts a low on the read/$\overline{\text{scan}}$ line, returning the keyboard control circuit to its normal mode of operation.

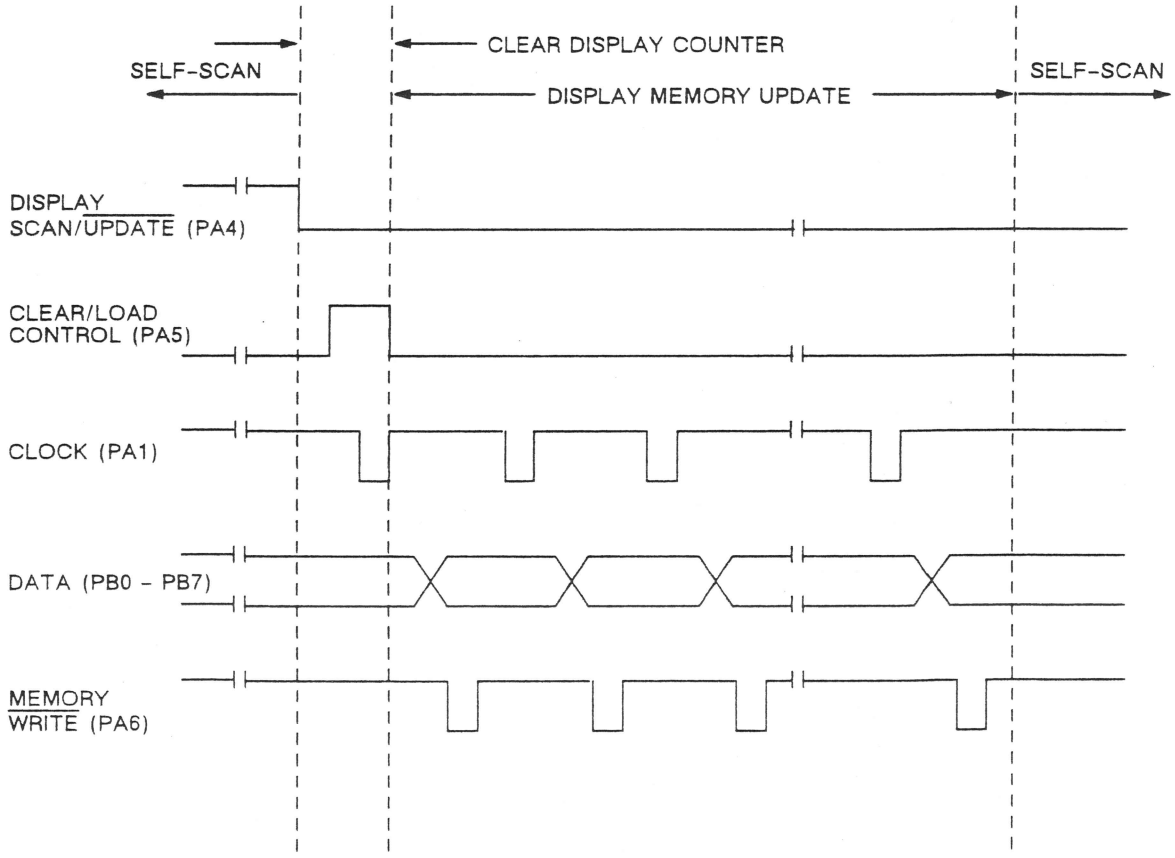



Figure 10-38. Memory Update Mode Sequence.

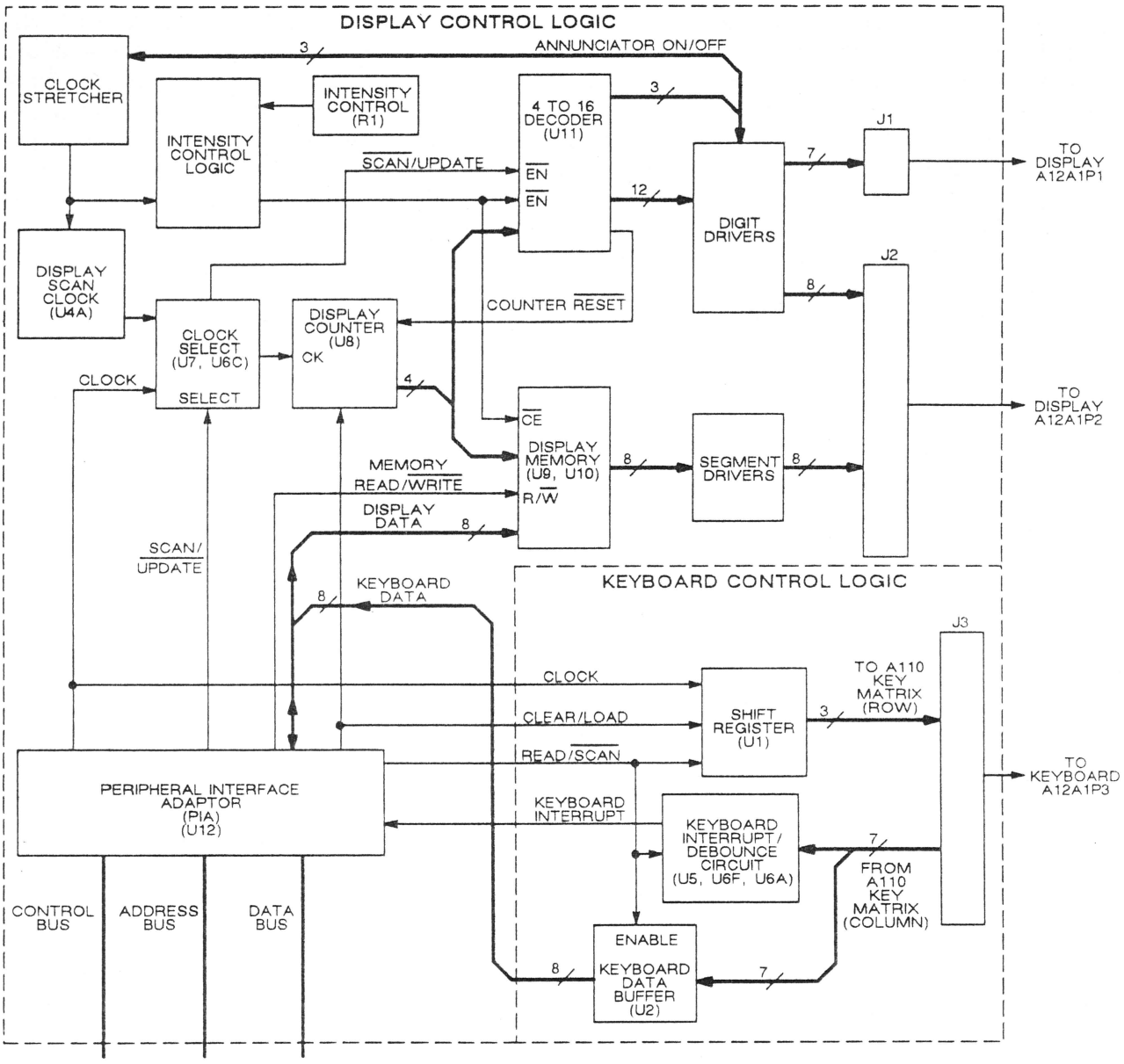



Figure 10-39. Front Panel Display Driver/Logic Functional Block Diagram.

## A12A2 FRONT PANEL DISPLAY DRIVER/LOGIC 2020419-01 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,DISC,CER | .002µF | 20% | 1KV | 2150005-00 | 2 |
| C2 | C1 | | | | | | |
| C3 | | CAP,TANTALUM | .1µF | 20% | 35V | 2300020-00 | 1 |
| C4 | | CAP,TANTALUM | 22µF | 20% | 16V | 2300030-00 | 1 |
| C5 | | CAP,TANTALUM | .33µF | 20% | 35V | 2300031-00 | 1 |
| C6 | | CAP,TANTALUM | 33µF | 20% | 10V | 2300015-00 | 1 |
| C7 | | CAP,SMD,CER,X7R | .01µF | 10% | 50V | 2100040-00 | 11 |
| C8 | C7 | | | | | | |
| C9 | C7 | | | | | | |
| C10 | C7 | | | | | | |
| C11 | C7 | | | | | | |
| C12 | C7 | | | | | | |
| C13 | C7 | | | | | | |
| C14 | C7 | | | | | | |
| C15 | C7 | | | | | | |
| C16 | C7 | | | | | | |
| C17 | C7 | | | | | | |
| CR1 | | DIODE,1N4148,FAST SWITCHING,GP | | | | 2704148-00 | 1 |
| J1 | | CONN,STRAIGHT PIN HDR,9 PIN | | | | 2610147-00 | 1 |
| J2 | | CONN,STRAIGHT PIN HDR,17 PIN | | | | 2610149-00 | 1 |
| J3 | | CONN,STRAIGHT PIN HDR,13 PIN | | | | 2610148-00 | 1 |
| P1 | | CONN,PCB,RT ANGLE,26 PIN | | | | 2620131-00 | 1 |
| Q1 | | XSTR,2N4124,NPN,GP | | | | 4704124-00 | 1 |
| Q2 | | XSTR,MPSD54,PNP,DARLINGTON | | | | 4710027-00 | 15 |
| Q3 | Q2 | | | | | | |
| Q4 | Q2 | | | | | | |
| Q5 | Q2 | | | | | | |
| Q6 | Q2 | | | | | | |
| Q7 | | XSTR,MPS-D55,PNP,RF AMPLIFIER | | | | 4710019-00 | 8 |
| Q8 | Q7 | | | | | | |
| Q9 | Q7 | | | | | | |
| Q10 | Q7 | | | | | | |
| Q11 | Q7 | | | | | | |
| Q12 | Q7 | | | | | | |
| Q13 | Q2 | | | | | | |
| Q14 | Q7 | | | | | | |
| Q15 | Q2 | | | | | | |
| Q16 | Q2 | | | | | | |
| Q17 | Q7 | | | | | | |
| Q18 | Q2 | | | | | | |
| Q19 | Q2 | | | | | | |
| Q20 | Q2 | | | | | | |
| Q21 | Q2 | | | | | | |
| Q22 | Q2 | | | | | | |
| Q23 | Q2 | | | | | | |
| Q24 | Q2 | | | | | | |
| R1 | | POT,CERMET,TO5 | 200K | .5W | 10% | 4250022-00 | 1 |
| R2 | | RES,CC | 2.4K | 1/4W | 5% | 4010242-00 | 1 |
| R3 | | RES,CC | 75K | 1/4W | 5% | 4010753-00 | 1 |
| R4 | | RES,CC | 220 | 1/4W | 5% | 4010221-00 | 1 |
| R5 | | RES,CC | 10K | 1/4W | 5% | 4010103-00 | 1 |
| R6 | | RES,CC | 390 | 1/4W | 5% | 4010391-00 | 1 |
| R7 | | RES,CC | 200 | 1/4W | 5% | 4010201-00 | 1 |

## A12A2 FRONT PANEL DISPLAY DRIVER/LOGIC (Continued) 2020419-01 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| R8 | | RES,CC | 15K | 1/4W | 5% | 4010153-00 | 1 |
| R9 | | NOT USED | | | | | |
| R10 | | NOT USED | | | | | |
| R11 | | NOT USED | | | | | |
| R12 | | RES,CC | 120K | 1/4W | 5% | 4010124-00 | 1 |
| R13 | | RES,SMD | 18.2 | 1/8W | 1% | 4231829-00 | 8 |
| R14 | R13 | | | | | | |
| R15 | R13 | | | | | | |
| R16 | R13 | | | | | | |
| R17 | R13 | | | | | | |
| R18 | R13 | | | | | | |
| R19 | R13 | | | | | | |
| R20 | R13 | | | | | | |
| R21 | | NOT USED | | | | | |
| R22 | | NOT USED | | | | | |
| R23 | | NOT USED | | | | | |
| R24 | | NOT USED | | | | | |
| R25 | | NOT USED | | | | | |
| R26 | | NOT USED | | | | | |
| R27 | | NOT USED | | | | | |
| R28 | | NOT USED | | | | | |
| R29 | | NOT USED | | | | | |
| R30 | | NOT USED | | | | | |
| R31 | | NOT USED | | | | | |
| R32 | | RES,CC | 39K | 1/4W | 5% | 4010393-00 | 3 |
| R33 | R32 | | | | | | |
| R34 | R32 | | | | | | |
| RN1 | | RES,NTWK | 9X10K | 0.2W | 2% | 4170003-00 | 3 |
| RN2 | RN1 | | | | | | |
| RN3 | RN1 | | | | | | |
| RP1 | | RES,NTWK,DIP | 8X1K | .3W | 2% | 4170031-00 | 2 |
| RP2 | RP1 | | | | | | |
| RP3 | | RES,NTWK,SMD | 8X220 | .3W | 2% | 4170032-00 | 1 |
| TP1 | | CONN,PCB,.040D PIN,GOLD | | | | 2620032-00 | 8 |
| TP2 | TP1 | | | | | | |
| TP3 | TP1 | | | | | | |
| TP4 | TP1 | | | | | | |
| TP5 | TP1 | | | | | | |
| TP6 | TP1 | | | | | | |
| TP7 | TP1 | | | | | | |
| TP8 | TP1 | | | | | | |
| U1 | | IC,SR,PRL ACCESS,4-BIT,TI ONLY | | | | 3084195-01 | 1 |
| U2 | | IC,74LS244 | | | | 3084244-00 | 1 |
| U3 | | IC,74LS132 | | | | 3084132-00 | 1 |
| U4 | | IC,74LS123 | | | | 3084123-00 | 1 |
| U5 | | IC,74LS30 | | | | 3087430-00 | 1 |
| U6 | | IC,74LS14 | | | | 3087414-00 | 1 |
| U7 | | IC,74LS51 | | | | 3087451-00 | 1 |
| U8 | | IC,74LS163 | | | | 3084163-00 | 1 |
| U9 | | IC,74LS189 | | | | 3057489-00 | 2 |
| U10 | U9 | | | | | | |
| U11 | | IC,74154 | | | | 3074154-00 | 1 |
| U12 | | IC,MC68B21P,PRPHL INTERFACE ADAPTER | | | | 3086821-00 | 1 |
| | | PCB SCHEMATIC DIAGRAM | | | | 5500419-00 D | REF. |

## Front Panel Display Driver/Logic Component Locator (PCB Assembly A12A2)

(See following page)

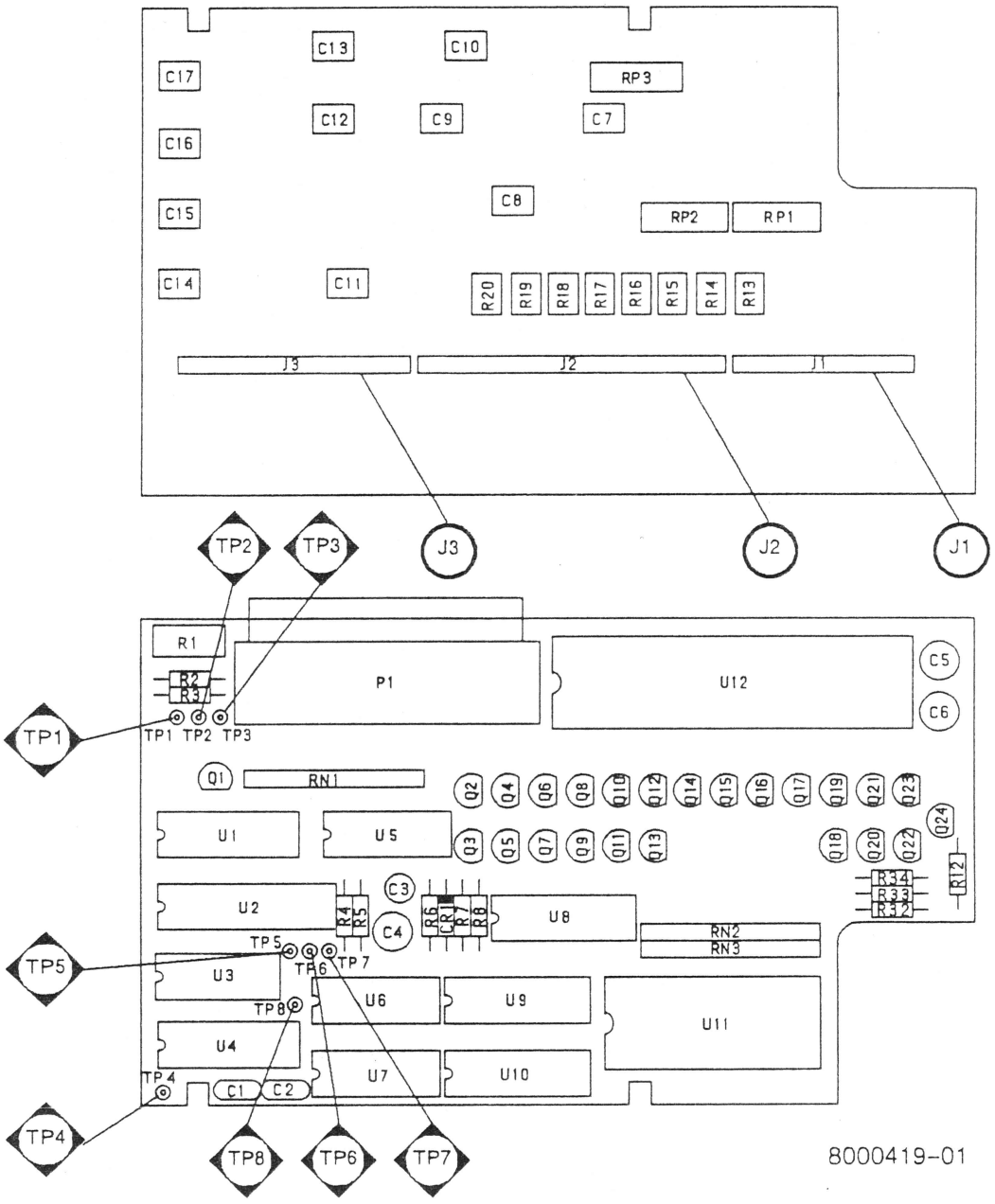



Figure 10-40. Front Panel Display Driver/Logic (A12A2) Component Locator.

UNUSED GATES

| MICROCIRCUIT ID CHART | | |
|---|---|---|
| DES | GND | +5V |
| U1 | 8 | 16 |
| U2 | 10 | 20 |
| U3 | 7 | 14 |
| U4 | 8 | 16 |
| U5 | 7 | 14 |
| U6 | 7 | 14 |
| U7 | 7 | 14 |
| U8 | 8 | 16 |
| U9 | 8 | 16 |
| U10 | 8 | 16 |
| U11 | 12 | 24 |
| U12 | 1 | 20 |

| LAST USED | NOT USED |
|---|---|
| C17 | |
| CR1 | |
| J3 | |
| P1 | |
| Q24 | |
| R20 | |
| RN3 | |
| RP3 | |
| TP8 | |
| U12 | |

2. ALL CAPACITORS ARE EXPRESSED IN MICROFARADS. ALL .01 CAPS ARE 100V.

1. ALL RESISTORS ARE 1\8W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500419-01

Figure 10-41. Front Panel Display Driver/Lo
(A12A2) Schematic Diagram.

# A13
# REAR PANEL
# 2010828-02

The Rear Panel assembly consists of the following:

- Metal mounting panel
- Ac power input receptacle
- Voltage selection switch
- Fuse assembly
- Fan assembly
- 10 MHz IN/OUT signal connector
- GPIB interface connector
- (Optional) 12 VDC input connector

The ac power receptacle accepts a standard 3-prong polarized plug.

The voltage selection switch allows the counter to operate on ac voltages of 100, 120, 140, 200, 220, or 240 volts.

The slow-blow fuse provides protection for the counter against excessive current.

The fan assembly houses an axial fan that circulates air to provide internal cooling for the counter.

The 10 MHz IN/OUT connector, a BNC (female) jack, provides the input for an external 10 MHz time base signal or, alternatively, the output for the counter's internal 10 MHz time base signal.

The GPIB (general purpose interface bus) connector, along with the associated internal circuitry, allows the counter to be operated remotely over the IEEE 488 interface bus.

The optional 12 VDC input connector provides an external input to power the oven oscillator (Option 05) during transit.

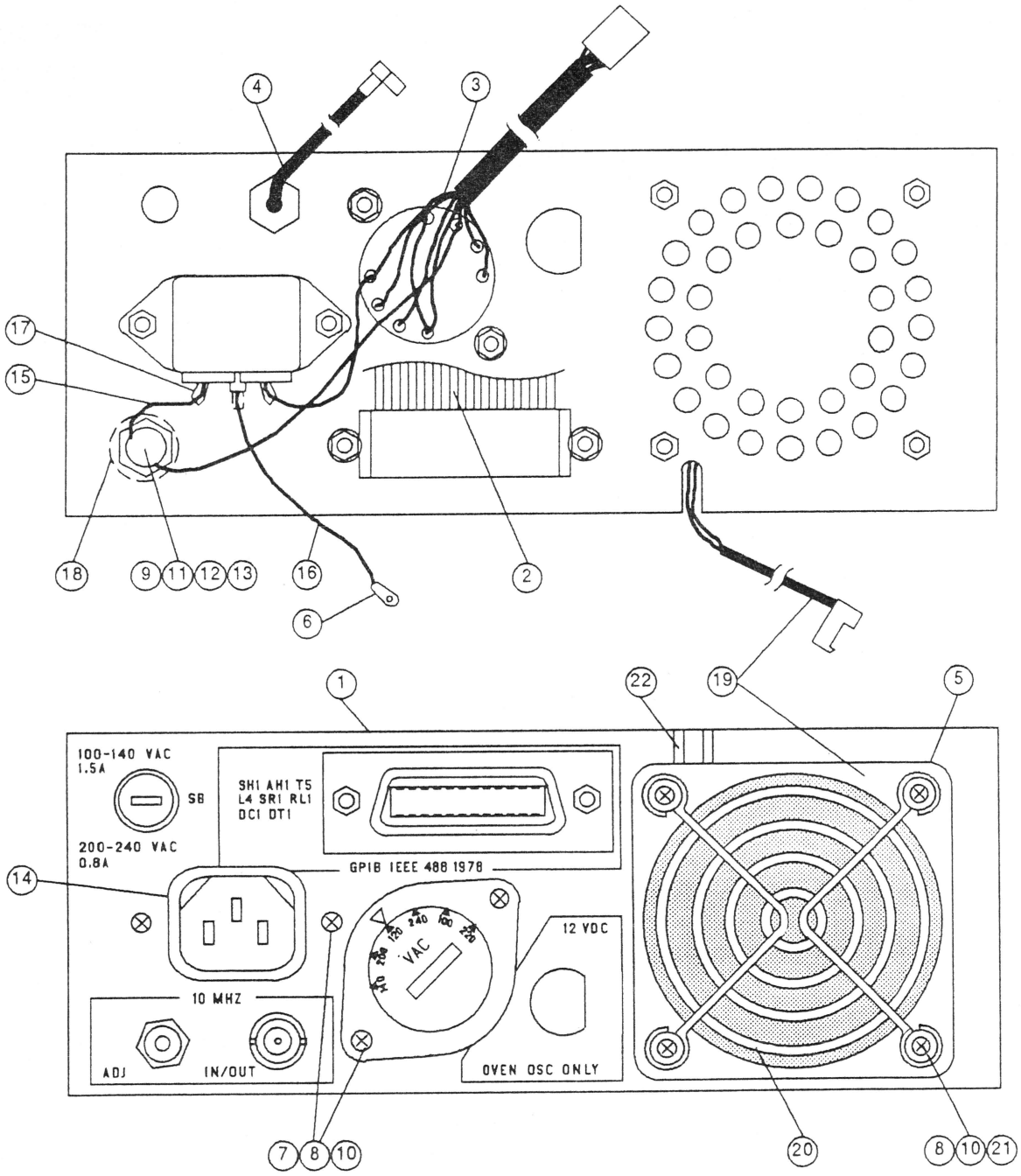



Figure 10-42. Rear Panel (A13).

## A13 REAR PANEL 2010828-02 Rev. B

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | PANEL,REAR | 5210845-01 | 1 |
| 2 | CABLE ASSY,FLAT RBN,GPIB | 2040469-01 | 1 |
| 3 | SWITCH ASSY,VOLT SELECT | 2010833-01 | 1 |
| 4 | CABLE ASSY,COAX,10 MHZ,I/O | 2040474-01 | 1 |
| 5 | SPACER,RND,.1151DX,.186DX,.750LG | 5110083-00 | 4 |
| 6 | SOLDER LUG,#4 | 5000049-00 | 1 |
| 7 | SCR,PNH X-REC 4-40 X 3/8 UNC | 5120004-06 | 4 |
| 8 | WASHER,FLAT,CRES NO.4 | 5160004-00 | 8 |
| 9 | WASHER,FIBER | 5000192-00 | 1 |
| 10 | NUT,HEX,SLFLKG,CRES 4-40 UNC-3B | 5184004-40 | 8 |
| 11 | FUSE,1.5AMP SB 3AG 250V | 5000101-00 | 1 |
| 12 | CARRIER,FUSE,3AG,GREY(DOM) | 5000171-00 | 1 |
| 13 | HOLDER,FUSE,W/MTG NUT | 5000170-00 | 1 |
| 14 | CONN,RCPT,PWR,W/FILTER | 2650013-00 | 1 |
| 15 | WIRE,INSUL,18AWG GRY | 5418888-00 | 6 |
| 16 | WIRE,INSUL,18AWG GRN | 5418555-00 | 3.5 IN. |
| 17 | TUBING,SHRINK,3/16 BLK | 5480011-00 | 1 |
| 18 | TUBING,SHRINK,3/4 BLK | 5480005-00 | 1.5 IN. |
| 19 | FAN ASSY | 2010855-01 | 1 |
| 20 | FAN,GUARD | 5000361-00 | 1 |
| 21 | SCR,PNH X-REC 4-40 X 1 3/8 UNC | 5120004-22 | 4 |
| 22 | GROMMET,CATERPILLAR,1/16" | 5000355-00 | 0.5 IN. |

# SECTION 11
# OPTIONS

This section provides a description, interconnection diagram, specifications, parts list, and a calibration procedure for the high-stability oven oscillator (Option 05).

| Option | Description | EIP P/N |
|---|---|---|
| 05 | High-stability Oven Oscillator | 2010874-01 |
| 14 | 2-year Warranty Extension (Total = 3 years) | 2010873-01 |

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# OPTION 05
# HIGH STABILITY OVEN OSCILLATOR
# (2010874-01)

## INTRODUCTION

The optional high stability oven oscillator improves counter measurement accuracy by minimizing frequency error caused by long-term frequency drift (aging rate), while providing both improved short-term stability and temperature stability. For the oven oscillator, the crystal is housed in a proportional control oven which maintains the crystal at an elevated temperature, reducing the effects of changes in ambient temperature on oscillator frequency output. The oven is energized whenever the counter line cord is connected to an ac power source, or when 12 V is input to the 12 VDC connector mounted on the rear panel of the counter.

## SPECIFICATIONS

| | |
|---|---|
| Aging rate per 24 hours (after 72 hours warm-up) | $<\|5 \times 10^{-10}\|$ |
| Short term stability (for 1 s averaging time) | $<1 \times 10^{-10}$ rms |
| 0° to +50° C temperature stability | $<\|3 \times 10^{-8}\|$ |
| ±10% line voltage change | $<\|2 \times 10^{-10}\|$ |
| Phase noise | -95 dBc/Hz at 10 Hz from carrier |
| Warm-up time | 72 hours |
| Retrace | $<\|5 \times 10^{-8}\|$ of final value 15 minutes after counter is plugged in at 25° C, if counter is unplugged for less than 10 minutes. |

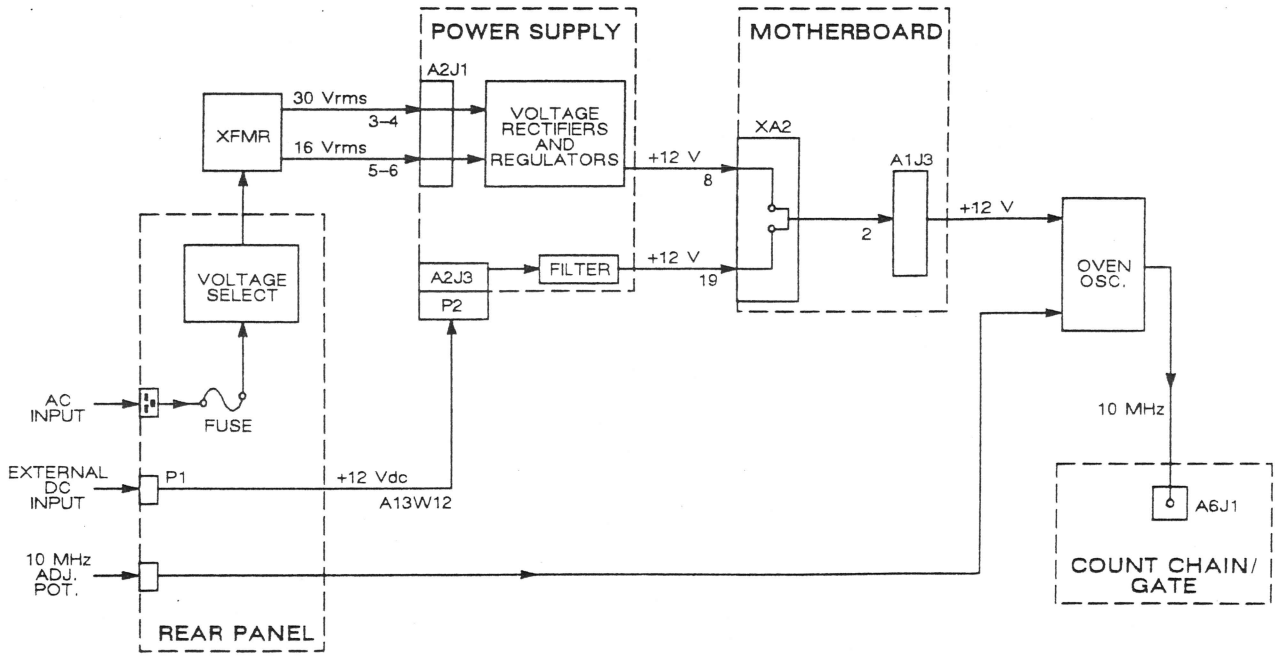


Fig 11-1. Oven Oscillator Block Diagram.

## POWER INPUT FOR THE OVEN OSCILLATOR

Whenever the line cord of the counter is connected to an ac power source, the power supply is energized and outputs, among other voltages, a regulated 12 V supply to power the oven oscillator. The regulated 12 V from the power supply is routed through the Motherboard and applied to the oven oscillator assembly.

To maintain the oscillator temperature during transit, the voltage supply for the oven oscillator can be applied at the 12 VDC input connector on the rear panel of the counter. From the rear panel, the 12 V oven supply is routed through a filtering network on the power supply, and through the Motherboard to the oven oscillator. A cable for connecting the 12 VDC input to an automobile cigarette lighter is included with the oven oscillator option.

## TIME BASE CALIBRATION

### DESCRIPTION

The accuracy of the oven oscillator directly affects the measurement accuracy of the 625A counter. From the time an oscillator is set to its specified frequency, it will begin drifting. The magnitude of the frequency drift is specified as the aging rate of the oscillator. Time base calibration removes the frequency error due to the aging rate of the oscillator. To maintain an accuracy of ±2 kHz on a 20 GHz measurement, calibration of the time base is recommended once every six months.

NOTE

Calibration of the time base should be made only after the oscillator has been continuously operated for a minimum of 72 hours, allowing for stabilization of the oscillator.

In the following procedure, the time base is calibrated against a frequency standard, using an oscilloscope. The 10 MHz frequency standard is used to trigger the oscilloscope while the 10 MHz signal from the counter is applied to channel 1 of the oscilloscope. Since the oscilloscope is triggered by the frequency standard, any difference in frequency between the 10 MHz frequency standard and the 10 MHz from the counter causes the displayed signal trace to move to the left or to the right. The rate of the signal trace movement is directly proportional to the frequency difference between the frequency standard and the time base in the counter. The fractional time base error can be calculated using the following formula:

$$\text{Fractional Time Base Error} = (\text{movement in cm per second}) \times (\text{time per division})$$

For example, if the sweep speed of the oscilloscope is set to 1 µs per division, and the signal is drifting at a rate of 2 cm per second, then the fractional time base error is calculated as follows:

$$\text{Fractional Time Base Error} = \frac{2\ \text{cm}}{\text{s}} \times \frac{1 \times 10^{-6}\ \text{s}}{\text{cm}} = 2 \times 10^{-6}$$

The actual time base error in Hz is calculated by multiplying the fractional time base error by the frequency of the frequency standard, as follows:

$$\text{Time Base Error (Hz)} = \pm[(2 \times 10^{-6}) \times (10 \times 10^{6})] = \pm 20\ \text{Hz}$$

The counter measurement error is calculated by multiplying the fractional time base error by the frequency of the signal being measured. For example, if the fractional time base error is $2 \times 10^{-6}$, then the measurement error on a 20 GHz signal is calculated as follows:

$$\text{Measurement Error (Hz)} = \pm[(2 \times 10^{-6}) \times (20 \times 10^{9})] = \pm 40\ \text{kHz}$$

## EQUIPMENT

Frequency standard (Stanford Research Systems FS700)
Oscilloscope (Tektronix 475)
50 ohm termination (Pamona 4119-50)

## EQUIPMENT SETUP

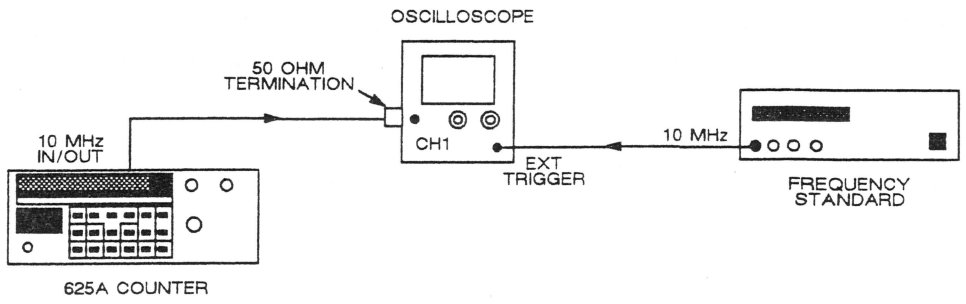


**Figure 11-2. Time Base Calibration Setup.**

## PROCEDURE

1. Turn on the EIP 625A counter and allow a warm-up period of at least 72 hours prior to calibrating the time base.

2. Set up the equipment as shown in Figure 11-2 and as described below.

3. Connect the frequency standard output to the external trigger input on the oscilloscope. Connect the 10 MHz IN/OUT connector from the rear panel of the 625A to the channel 1 input of the oscilloscope.

4. Set the oscilloscope to external trigger.

5. Set the oscilloscope sweep speed to 0.01 μs per cm.

6. While monitoring the 10 MHz time base signal from the 625A on the oscilloscope, adjust the frequency of the time base (by turning the rear panel 10 MHZ ADJ control) until the horizontal movement rate is ≤1 centimeter in 10 seconds. This sets the time base to an accuracy of $1 \times 10^{-9}$ (10 MHz ±50 mHz).

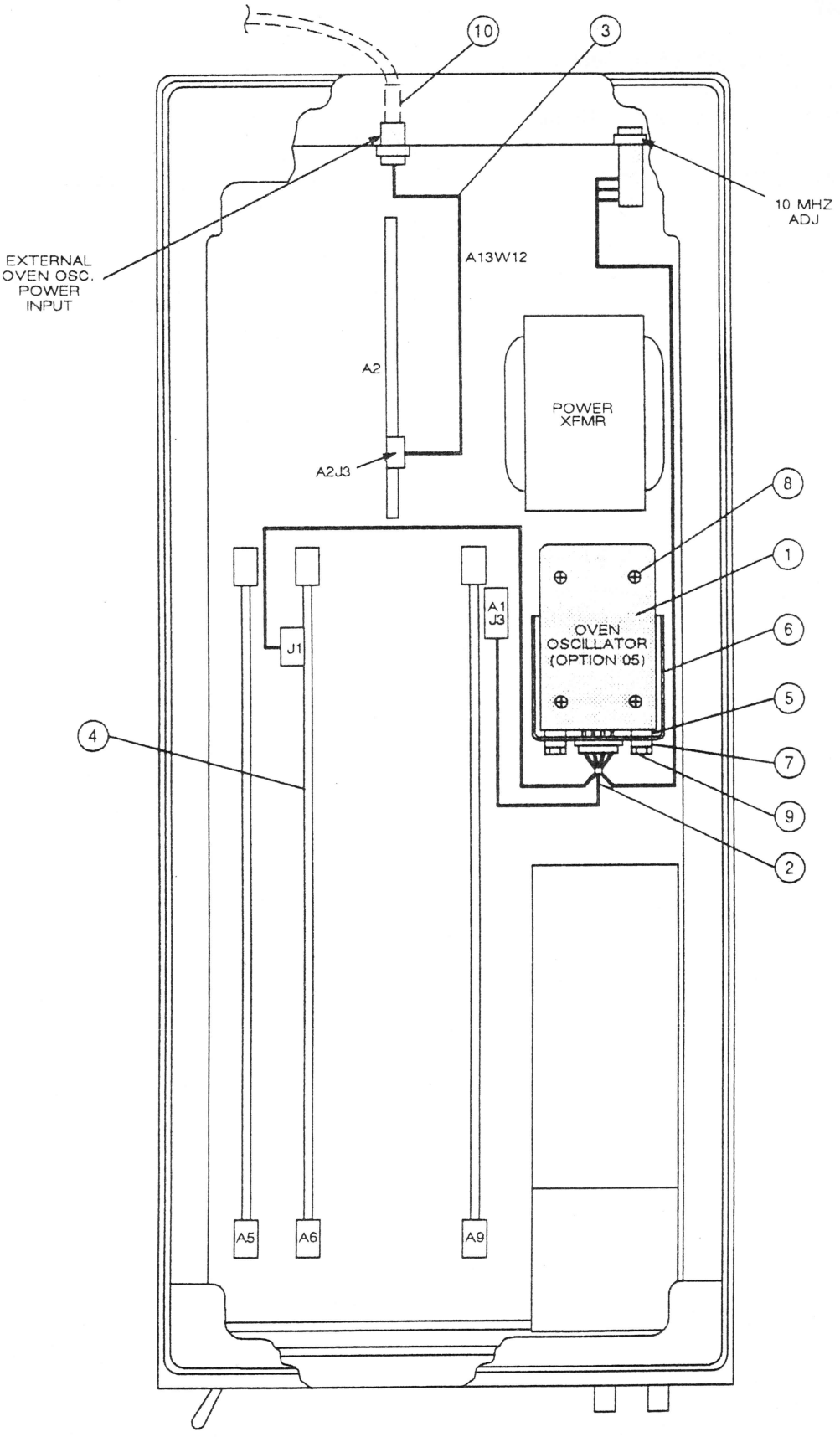


Figure 11-3. Oven Oscillator Interconnection Diagram.

## OPTION 05 HIGH-STABILITY OVEN OSCILLATOR 2010874-01 Rev. B

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | OSC,OVEN,5X10-10,OPT 05,12V | 2030143-01 | 1 |
| 2 | HARNESS ASSY,TIMEBASE | 2010857-02 | 1 |
| 3 | CABLE ASSY,OVEN OSC HEATER,A13W12 | 2040467-02 | 1 |
| 4 | PCB ASSY,COUNT CHAIN/GATE,OVEN OSC | 2020421-04 | 1 |
| 5 | WASHER,FLAT,CRES NO.6 | 5160006-00 | 8 |
| 6 | BRACKET,MTG OVEN OSC | 5210902-01 | 1 |
| 7 | GROMMET,RUBBER | 5000017-00 | 4 |
| 8 | SCR,PNH X-REC SLFLKG 6-32X3/8 UNC | 5124006-06 | 4 |
| 9 | NUT,HEX,SLFLKG,CRES 6-32 UNC-3B | 5184006-32 | 4 |
| 10 | CABLE ASSY,OVEN OSC,12V EXT POWER | 2040489-01 | 1 |

**NOTE**

PCB assembly 2020421-04, item number 4 on the above parts list, replaces PCB assembly 2020421-03 (A6) when the optional oven oscillator is installed. PCB 2020421-04 is identical to 2020421-03 with the following exceptions:

- TCXO Y1 is not installed on 2020421-04.
- Capacitor C1 is not installed on 2020421-04.
- Connector J1 is installed on 2020421-04.

A portion of the schematic of the Count Chain/Gate (A6) circuitry is illustrated below, showing the modifications performed when the oven oscillator option is installed.

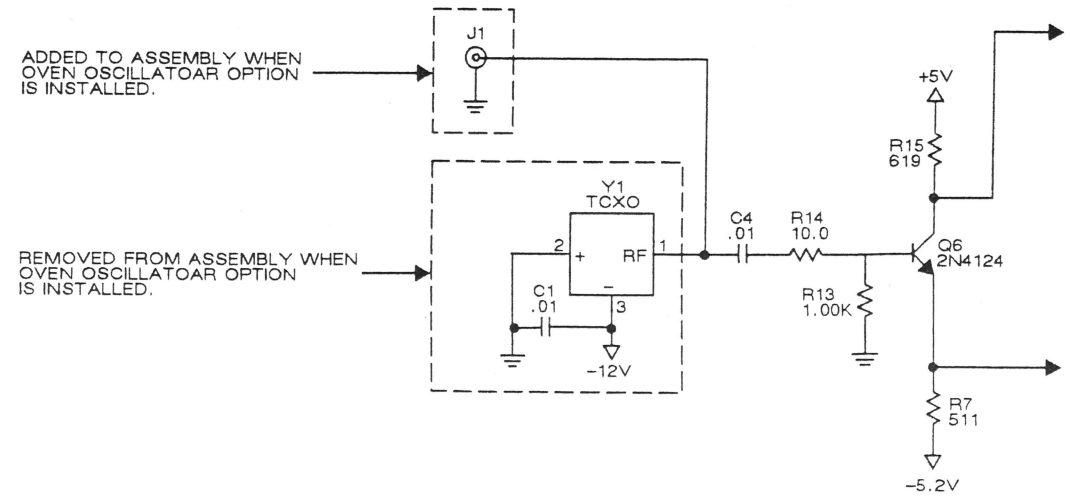


Figure 11-4. Count Chain/Gate Modifications for Option 05.

# APPENDIX A
# ACCESSORIES

| Accessory | Description | EIP P/N |
|---|---|---|
| 011 | Rack Mount Kit for one EIP 625A* | 2010892-01 |
| 012 | Rack Mount Kit for two EIP 625A units (side-by-side) | 2010893-01 |
| 013 | Rack Mount Kit for one EIP 625A and one HP 3 1/2" Systems II 1/2 rack module (side-by-side) | 2010894-01 |
| 014 | Rack Mount Kit for one EIP 625A and one Wavetek model 8531 Power Meter or one Marconi model 6960 Power Meter (side-by-side) | 2010895-01 |
| 015 | Rack Mount Kit for one EIP 625A and one Boonton model 4220 Power Meter (side-by-side) | 2010896-01 |
| 016 | Chassis Slide Kit for one EIP 625A* | 2010889-01 |
| 017 | Chassis Slide Kit for two EIP 625A | 2010888-01 |
| 021 | Transit Case for 625A Counter | 5700005-00 |
| 031 | Extra Operating Manual (one supplied at no charge with instrument) | 5585043-00 |
| 032 | Service Manual | 5585035-01 |
| 042 | Service Kit | 2010891-01 |

* See drawings.

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## ACCESSORY 011 - RACK MOUNT KIT FOR ONE EIP 625A 2010892-01 Rev. A

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | RACK MOUNT W/O HANDLES,GRAY,3.50IN | 5210433-12 | 1 |
| 2 | ADAPTER PLATE,RACK MTG | 5210870-01 | 1 |
| 3 | NUT,FLANGE,8-32 | 5210441-01 | 4 |
| 4 | SCR,FLH X-REC,(100)SLFLKG,8-32X5/16 UNC | 5149001-05 | 2 |
| 5 | SCR,PNH X-REC, SLFLKG 8-32X5/16 UNC | 5124008-05 | 2 |
| 6 | SCR,PNH X-REC,10-32X7/16 UNF | 5120010-57 | 4 |

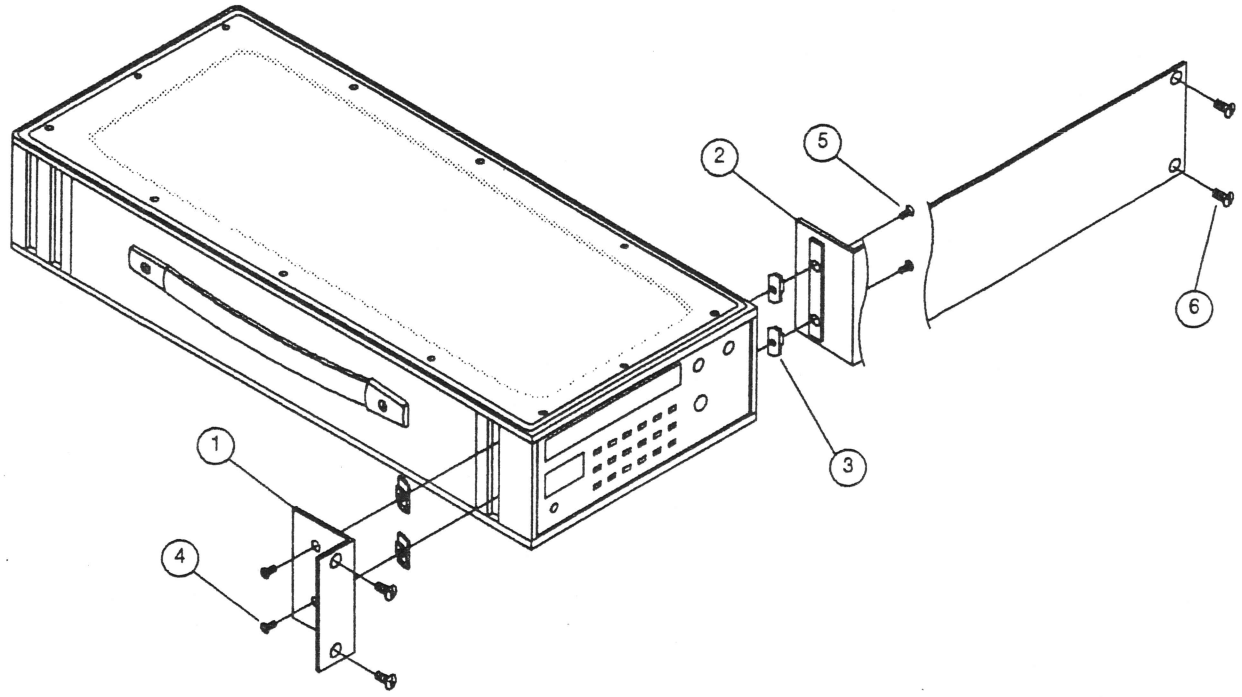


Figure A-1. Accessory 011 - Rack Mount Kit for One EIP 625A.

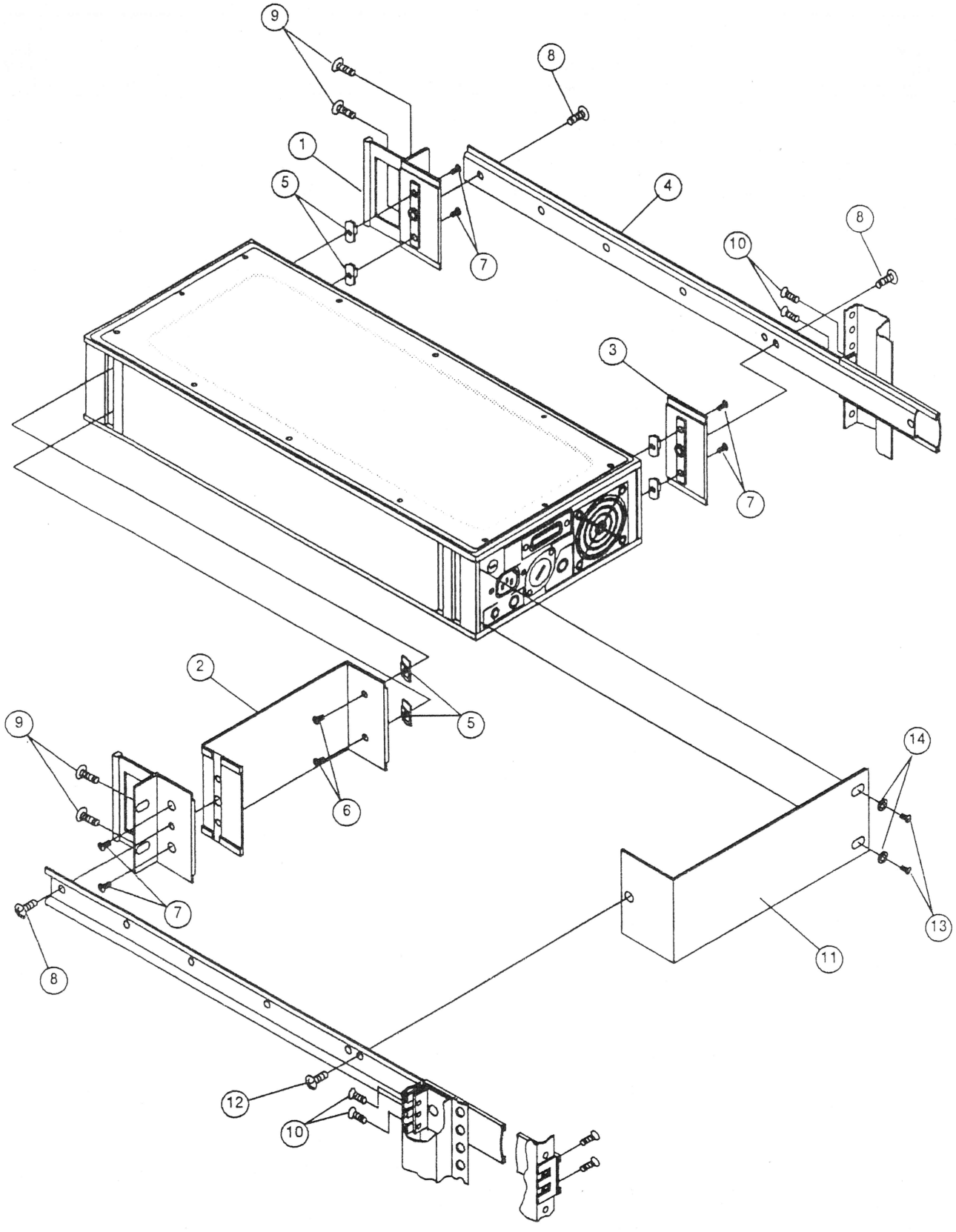


Figure A-2. Accessory 016 - Chassis Slide Kit for One EIP 625A.

## ACCESSORY 016 - CHASSIS SLIDE KIT FOR ONE EIP 625A 2010889-01 Rev. A

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | RACK MOUNT W/HANDLES,D GRAY,3.50 IN | 5210435-12 | 2 |
| 2 | ADAPTER PLATE,SLIDE MTG | 5210924-01 | 1 |
| 3 | SPACER,REAR CORN POST,2U 3.5 | 5210434-02 | 1 |
| 4 | CHASSIS SLIDE,MODIF | 2010928-01 | 2 |
| 5 | NUT,FLANGE,8-32 | 5210441-01 | 6 |
| 6 | SCR,PNH X-REC,SLFLKG 8-32X5/16 UNC | 5124008-05 | 2 |
| 7 | SCR,FLH X-REC,(100) SLFLKG,8-32X5/16 UNC | 5149001-05 | 6 |
| 8 | SCR,PNH X-REC,SLFLKG 8-32X1/4 UNC | 5124008-04 | 3 |
| 9 | SCR,PNH X-REC,10-32X7/16 UNF | 5120010-57 | 4 |
| 10 | SCR,FLH X-REC 10-32X7/16 UNF | 5140010-57 | 4 |
| 11 | BRACKET,REAR,SLIDE MTG | 5210945-01 | 1 |
| 12 | SCR,PNH X-REC,10-32X1/2 UNF | 5120010-58 | 1 |
| 13 | SCR,PNH X-REC,SLFLKG 6-32X5/16 UNC | 5124006-05 | 2 |
| 14 | WASHER,FLAT,CRES NO. 6 | 5160006-00 | 2 |

# QUICK REFERENCE LIST OF GPIB COMMAND MESSAGES

## CONTROL MESSAGES

| Header | Argument | Terminator | Description |
|---|---|---|---|
| CLEARDISPLAY | None | None | Returns the display to measurement results display, clears errors (equivalent to front panel CLEAR DISPLAY key). |
| INITIALIZE | " | " | Reconfigures the instrument to power-up state. |
| RESET | " | " | Resets counter to restart a new signal acquisition (equivalent to front panel key). |
| TRIGGER | " | " | Triggers a new measurement cycle (equivalent to front panel "."key). |

## MODE MESSAGES

| Header | Argument | Terminator | Description |
|---|---|---|---|
| DYNAMIC | ON or OFF | None | Suppresses blanks when counter is configured in talker mode for faster free-field data transfer. |
| EXTERNAL | " | " | Controls the INT/EXT time base reference. (Special Function 08 can also be used to select the external time base.) |
| HEADER | " | " | Adds an alpha header and terminator for talker. |
| HOLD | " | " | Holds the last result if on. |
| SCIENTIFIC | " | " | Selects scientific notation for talker. |

## PARAMETER MESSAGES

| Header | Argument | Terminator | Description |
|---|---|---|---|
| ASRQMASK | <number> | None | Selects the ANDed combination of status events to cause a service request. |
| BAND | " | " | Selects a specific band (1 to 3) or DEFAULT. |
| CENTERFREQ | " | (Hz/kHz/MHz/GHz) | Sets a center frequency value and mode. |
| FETCH | " | None | Recalls counter setup stored in specified storage register (0 to 9) (see Special Function 73). |
| MEMORY | <hex_adrs> | <hex_data> | Accesses a memory location and alters it (altering is optional). |
| MEMORY | INCREMENT | " | Accesses the next location and alters it (altering is optional). |
| MEMORY | DECREMENT | " | Accesses the previous location and alters it (altering is optional). |
| MULTIPLIER | " | None | Inputs a multiplier value (01 to 99). |
| OFFSETFREQ | " | (Hz/kHz/MHz/GHz) | Sets a frequency offset value (1 kHz to 99.9 GHz). |
| RESOLUTION | " | None | Sets the frequency measurement resolution (0 to 9) (also .1 in Band 1 only). |
| SAMPLERATE | " | (s/ms) | Sets a delay between measurement values (0 to 100 sec, 10 ms resolution). |
| SPECIAL | " | None | Activates a specific special function (01 to 99). |
| SRQMASK | " | " | Selects the ORed combination of status events to cause a service request. |
| STORE | " | " | Stores current counter setup in specified storage register (0 to 9) (see Special Function 72). |
| V1FREQ | " | (Hz/kHz/MHz/GHz) | Sets a start frequency for VCO sweep (see Special Functions 41, 42). |
| V2FREQ | " | " | Sets a stop frequency for VCO sweep (see Special Functions 41, 42). |

## QUICK REFERENCE LIST OF GPIB COMMAND MESSAGES (Continued)

### PARAMETER MESSAGES (Continued)

| Header | Argument | Terminator | Description |
|---|---|---|---|
| Y1FREQ | " | " | Sets a start frequency for YIG sweep (See Special Function 40).s |
| Y2FREQ | " | " | Sets a stop frequency for YIG sweep (see Special Function 40). |
| Y3FREQ | " | " | Sets YIG frequency (see Special Function 20). |

### OUTPUT CONTROL MESSAGES

| Command | Description |
|---|---|
| OUTPUT BAND | Outputs the number of the last specified band. |
| OUTPUT CENTERFREQ | Outputs the center frequency last specified. |
| OUTPUT DATE | Outputs a 25-character string that shows the EIP part number, revision level, and date of the instrument firmware contained in the PROM on the microprocessor assembly. |
| OUTPUT ERRORNUMBER | Outputs the number of the last error (see listing of error numbers on page 3-20). |
| OUTPUT IDENTIFICATION | Outputs "EIP625A GPIB dd", where dd is the two-digit GPIB address. |
| OUTPUT KEYCODE | Outputs the code of the last key pressed. |
| OUTPUT LEVEL | Outputs a number between 0 and 8 corresponding to the signal level applied to Band 3 (see Special Function 20). |
| OUTPUT MEMORY | Outputs the contents of the memory in the last accessed location. |
| OUTPUT MULTIPLIER | Outputs the last specified multiplier value. |
| OUTPUT OFFSETFREQ | Outputs the current offset frequency. |
| OUTPUT RESOLUTION | Outputs the last specified frequency measurement resolution. |
| OUTPUT SAMPLERATE | Outputs the last specified delay time between measurement values. |
| OUTPUT SETUP | Outputs a 106-character string that describes the current setup (see page 4-5.) |
| OUTPUT SRQMASK | Outputs the combination of status events required to cause a service request (see page 4-8). |
| OUTPUT V1FREQ | Outputs the last specified start frequency for VCO sweep (see Special Functions 41 and 42). |
| OUTPUT V2FREQ | Outputs the last specified stop frequency for VCO sweep (see Special Functions 41 and 42. |
| OUTPUT Y1FREQ | Outputs the last specified start frequency for YIG sweep (see Special Functions 40). |
| OUTPUT Y2FREQ | Outputs the last specified stop frequency for YIG sweep (see Special Functions 40). |
| OUTPUT Y3FREQ | Outputs the last specified YIG frequency (see Special Function 20). |

Dear Customer,

EIP welcomes any suggestions you may have for changes, additions, or corrections that would improve the usefulness of this manual. Your suggestions are a valuable part of the input used in revising our manuals and developing the structure and format of new ones.

Please send us your comments. Your contributions will help us attain our goal of providing you with the best possible service for your instrument.

Sales and Marketing
EIP Microwave, Inc.

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Instrument Model Number _____

Manual Publication Date _____

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# MANUAL BACKDATE

**MODEL:** EIP 625A

**MANUAL BACKDATE PART NO.:** 5580076-00, Rev. A
**CHANGE DATE:** October 25, 1990

## Manual Backdate Information

This manual backdate contains new information for the manual to reflect changes in the instrument that have occurred since the manual was published.

Title: Models 625A CW Microwave Counter, Operation and Service
Manual Assembly Part Number: 5585035-01
Manual Text Part Number: 5580075-01
Printing Date: October 1990
CCN: 8004

Before making the following changes, be sure to check the cover page of your manual and verify that the part numbers and printing date match the information given above. If it does not, contact EIP Microwave, Inc. or your local EIP sales representative for assistance.

The changes contained herein are based on the CCN (configuration control number) of your instrument, listed on the rear frame of the instrument. This backdate provides information to backdate the manual from CCN: 8004 to CCN: 8002.

Verify that your instrument was manufactured at CCN: 8002 before proceeding with the following changes.

## Required Changes

Change CCN listing on front cover as follows:

Was: CCN 8004 Is: CCN 8002

The attached replacement pages are to be inserted into your manual per the following table.

| Existing Pages | Replace With |
|---|---|
| 10-3 through 10-4 | 10-3 through 10-4 |
| 10-11 through 10-24 | 10-11 through 10-24 |
| 10-35 through 10-36 | 10-35 through 10-36 |
| 10-43 through 10-54 | 10-43 through 10-54 |
| 10-63 through 10-74 | 10-63 through 10-74 |

## TOP ASSEMBLY 2000080-02

| ITEM NO. | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|
| 1 | PANEL ASSY,FRONT,625A | 2010829-02 | 1 |
| 2 | PANEL ASSY,REAR | 2010828-02 | 1 |
| 3 | XMFR ASSY,PWR | 2010832-01 | 1 |
| 4 | FRAME | 5210835-00 | 2 |
| 5 | CARD CAGE ASSY | 2010824-02 | 1 |
| 6 | PCB ASSY,MOTHERBOARD | 2020418-02 | 1 |
| 7 | PROM,PROGRAMMED,625A,PROCESSOR | 2060059-01 | 1 |
| 8 | POST,COR,FR,GRAY,2.70 | 5210430-12 | 2 |
| 9 | POST,CORNER,REAR | 5210863-01 | 2 |
| 10 | PANEL SIDE | 5210854-02 | 1 |
| 11 | PANEL SIDE,VENTED | 5210855-02 | 1 |
| 12 | SCR,PNH X-REC SLFLKG 4-40X5/16 UNC | 5124004-05 | 8 |
| 13 | SCR,PNH X-REC SLFLKG 6-32X3/8 UNC | 5124006-06 | 16 |
| 14 | SCR,PNH X-REC SLFLKG 8-32X1/2 UNC | 5124008-08 | 16 |
| 15 | SCR,FLH,X-REC 100DEG 6-32X5/16 UNC | 5140006-05 | 24 |
| 16 | SCR,PNH,X-REC,SEMS,INTL,4-40X3/8 | 5171004-06 | 1 |
| 17 | NUT,HEX,SLFLKG,CRES 4-40 UNC-3B | 5184004-40 | 1 |
| 18 | SCR,PNH X-REC SLFLKG 6-32X5/8 UNC | 5124006-10 | 2 |
| 19 | STANDOFF,1/4 HEX,6-32 X 2.590 LG | 5100106-00 | 3 |
| 20 | SCR,PNH X-REC SLFLKG 6-32X1/2 UNC | 5124006-08 | 3 |
| 21 | PCB ASSY,POWER SUPPLY | 2020417-02 | 1 |
| 22 | PCB ASSY,PROCESSOR,SER/PAR | 2020416-01 | 1 |
| 23 | PCB ASSY,COUNT CHAIN/GATE | 2020421-01 | 1 |
| 24 | CONVERTER ASSY,B3 | 2010864-01 | 1 |
| 25 | CABLE ASSY,FLAT RBN,F/P LOGIC | 2040169-01 | 1 |
| 26 | TIE,CABLE 0-4.00 ID | 5000266-00 | 1 |
| 27 | LABEL SET,PCB | 5560287-01 | 1 |
| 28 | COMPOUND,THERMAL | 5602004-00 | 1 |
| 29 | WASHER,FINISHING,.635ID | 5210382-02 | 1 |
| 30 | SCR,PNH X-REC SLFLKG 6-32X1/4 UNC | 5124006-04 | 6 |
| 31 | SCR,PNH X-REC SLFLKG 8-32X3/8 UNC | 5124008-06 | 1 |
| 32 | WASHER,FLAT,CRES NO.8 | 5160008-00 | 1 |
| 33 | PCB ASSY,SIGNAL CONDITIONER | 2020420-02 | 1 |
| 34 | CABLE ASSY,COAX,W9 | 2040475-01 | 1 |
| 35 | CABLE ASSY,COAX,W8 | 2040457-01 | 1 |
| 36 | CABLE ASSY,COAX,W7 | 2040486-01 | 1 |
| 37 | CABLE ASSY,COAX,W3 | 2040455-01 | 1 |
| 38 | CABLE ASSY,COAX,W10 | 2040473-01 | 1 |
| 39 | COVER ASSY,TOP | 2010886-01 | 1 |
| 40 | COVER ASSY,BOTTOM | 2010826-01 | 1 |
| 41 | LABEL, SER.NO. | 5560165-00 | 1 |
| 42 | LABEL,CALIBRATION | 5560180-00 | 1 |
| 43 | LABEL,OPTIONS | 5560181-00 | 1 |
| 44 | HANDLE,FLAT,FLEXIBLE | 5250035-00 | 1 |
| 45 | HANDLE ASSY,REMOVABLE,D GRAY,3.50 | 2010402-12 | 2 |
| 46 | GROMMET,CATERPILLAR,1/16" | 5000355-00 | 3 |
| 47 | BUTTON,PLUG,SS-51034 | 5000246-02 | 2 |
| 48 | FOOT,MOLDED,DP GRAY | 5220003-02 | 4 |
| 49 | PAD, RUBBER, FOOT | 5220002-00 | 4 |
| 50 | SCR,SLFLKG, FOOT 8-18X3/8 | 5000095-00 | 8 |
| | CORD,LINE 3-COND | 5440002-00 | 1 |
| | MANUAL ASSY,625A,OPERATION | 5585043-00 | 1 |

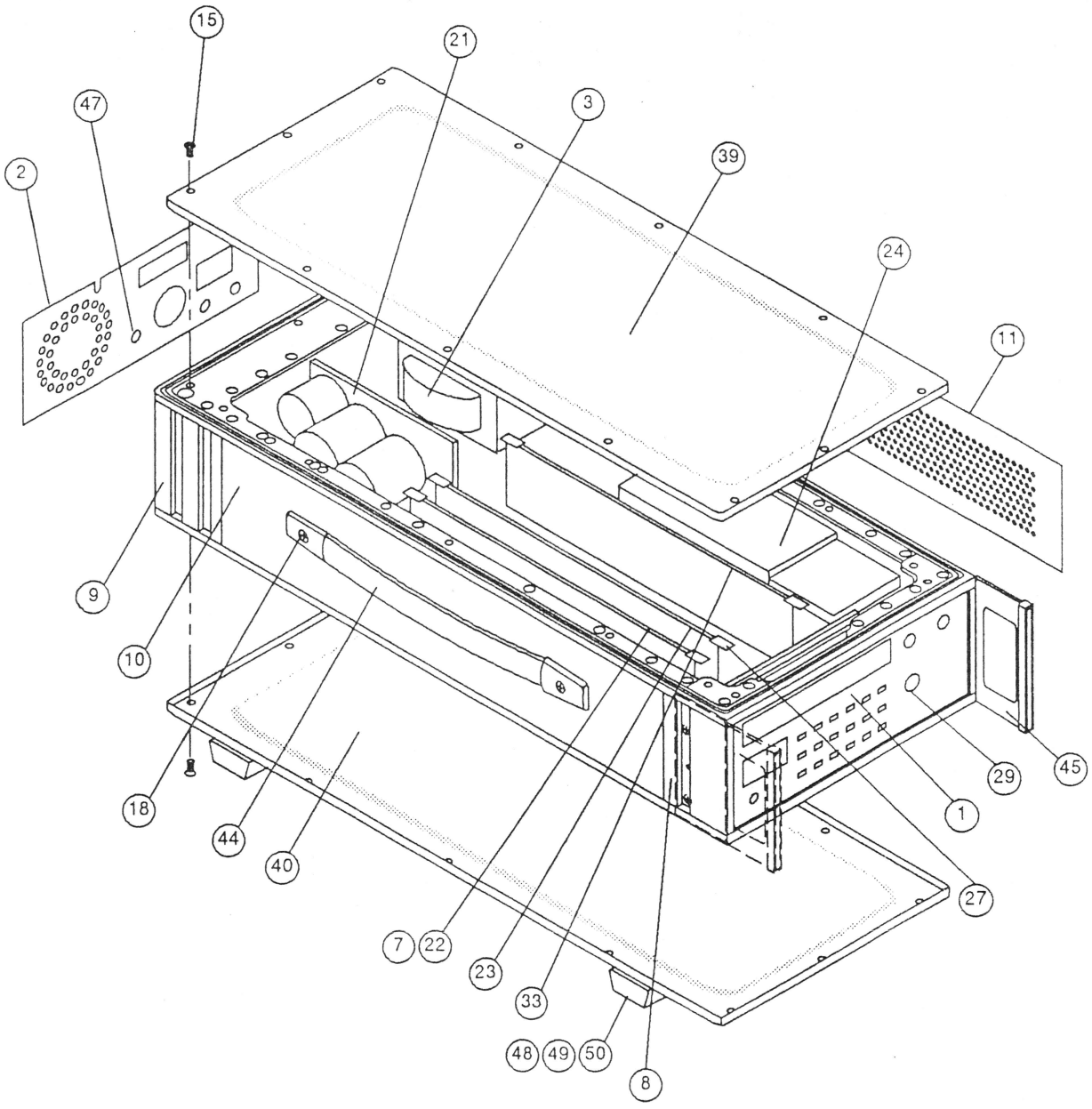


Figure 10-1. Top Assembly, Exploded View.

## A1
## MOTHERBOARD
## (2020418-02)

The primary purpose of the Motherboard assembly is to provide an electrical interface between the various sub-assemblies used in the counter. The Motherboard also contains a +5 volt regulator, a relay, and the circuitry used to control the speed of the fan.

The voltage regulator circuit, consisting of U1, C6 and C7, provides a separate +5 volt supply used to power the front panel display. The front panel display uses a separate dc supply to prevent digital noise, generated by the display, from interfering with the sensitive circuits used in the counter.

The relay is used to disconnect all dc voltages from the counter in the standby mode while still providing dc to the optional oven oscillator.

A fan control circuit varies fan speed as a function of the internal counter temperature. A thermistor is used to sense the internal temperature of the counter. As the temperature increases, the resistance of the thermistor decreases causing the voltage on the base of Q2 to increase. The increased voltage on the base of Q2 causes it to conduct harder which in turn causes Q1 to conduct harder, increasing fan speed and internal airflow. The value of resistor R4 determines the minimum fan speed.

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## A1 MOTHERBOARD 2020418-02 Rev. A

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,ELCTLT | 220µF | 20% | 35V | 2200033-00 | 2 |
| C2 | | CAP,DISC,CER | .1µF | | 50V | 2150092-00 | 1 |
| C3 | | CAP,TANTALUM | 47µF | 20% | 16V | 2300025-00 | 1 |
| C4 | | CAP,CER | .001µF | 20% | 100V | 2150001-00 | 1 |
| C5 | C1 | | | | | | |
| C6 | | CAP,TANTALUM | 10µF | 20% | 25V | 2300029-00 | 2 |
| C7 | C6 | | | | | | |
| J1 | | CONN,PCB HEADER,26 PIN,W/EJCTR | | | | 2620078-00 | 2 |
| J2 | J1 | | | | | | |
| J3 | | CONN,FRICT LK 156,6 PIN | | | | 2620090-00 | 1 |
| J4 | | NOT USED | | | | | |
| J5 | | CONN,FRICT LK,HEADER,.156 13 PIN | | | | 2620151-00 | 1 |
| J6 | | CONN,PC,RCPT LK 156,3 PIN | | | | 2620201-00 | 2 |
| J7 | J6 | | | | | | |
| K1 | | RELAY,PWR,6PDT,12V | | | | 3900007-00 | 1 |
| Q1 | | XSTR,MJE520,NPN,PWR | | | | 4710003-00 | 1 |
| Q2 | | XSTR,2N4401,NPN,SW AND AMP | | | | 4704401-00 | 1 |
| R1 | | RES,CC | 5.1 | 1/4W | 5% | 4010519-00 | 1 |
| R2 | | RES,CC | 1.1K | 1/4W | 5% | 4010112-00 | 1 |
| R3 | | THERMISTOR CHIP | | | | 4340005-00 | 1 |
| R4 | | RES,CC | 240 | 1W | 5% | 4030240-00 | 1 |
| R5 | | RES,M/OX | 2.74K | 1/10W | 1% | 4052741-00 | 1 |
| R7 | | RES,M/OX | 1.50K | 1/8W | 1% | 4061501-00 | 1 |
| U1 | | IC,7805C,VOLT RGLTR,+5V,TO-220 | | | | 3057805-02 | 1 |
| XA2 | | CONN,PCB EDGE,AMPL,11 PIN | | | | 2620183-00 | 1 |
| XA5 | | CONN,PCB EDGE,2 X 30 PIN,.125 X.250 | | | | 2610150-00 | 3 |
| XA6 | XA5 | | | | | | |
| XA7 | | NOT USED | | | | | |
| XA8 | | NOT USED | | | | | |
| XA9 | XA5 | | | | | | |

HARDWARE USED IN THIS ASSEMBLY

| | | | |
|---|---|---|---|
| | SCR,PNH,X-REC,SEMS,INTL,4-40X3/8 | 5171004-06 | 2 |
| | NUT,HEX,CRES 4-40 UNC-2B | 5180004-40 | 2 |
| | HEATSINK,VERT PCB MT,TO-220 | 5000363-00 | 1 |
| | SCR,PNH,X-REC,SEMS,INTL,4-40X1/4 | 5171004-04 | 1 |
| | WASH,LK,INTL-T,CRES # 4 | 5163004-00 | 2 |
| | PAD,INSULATOR,SILICON TO-126 | 5000236-00 | 1 |
| | PCB SCHEMATIC DIAGRAM | 5500418-02 A | REF. |

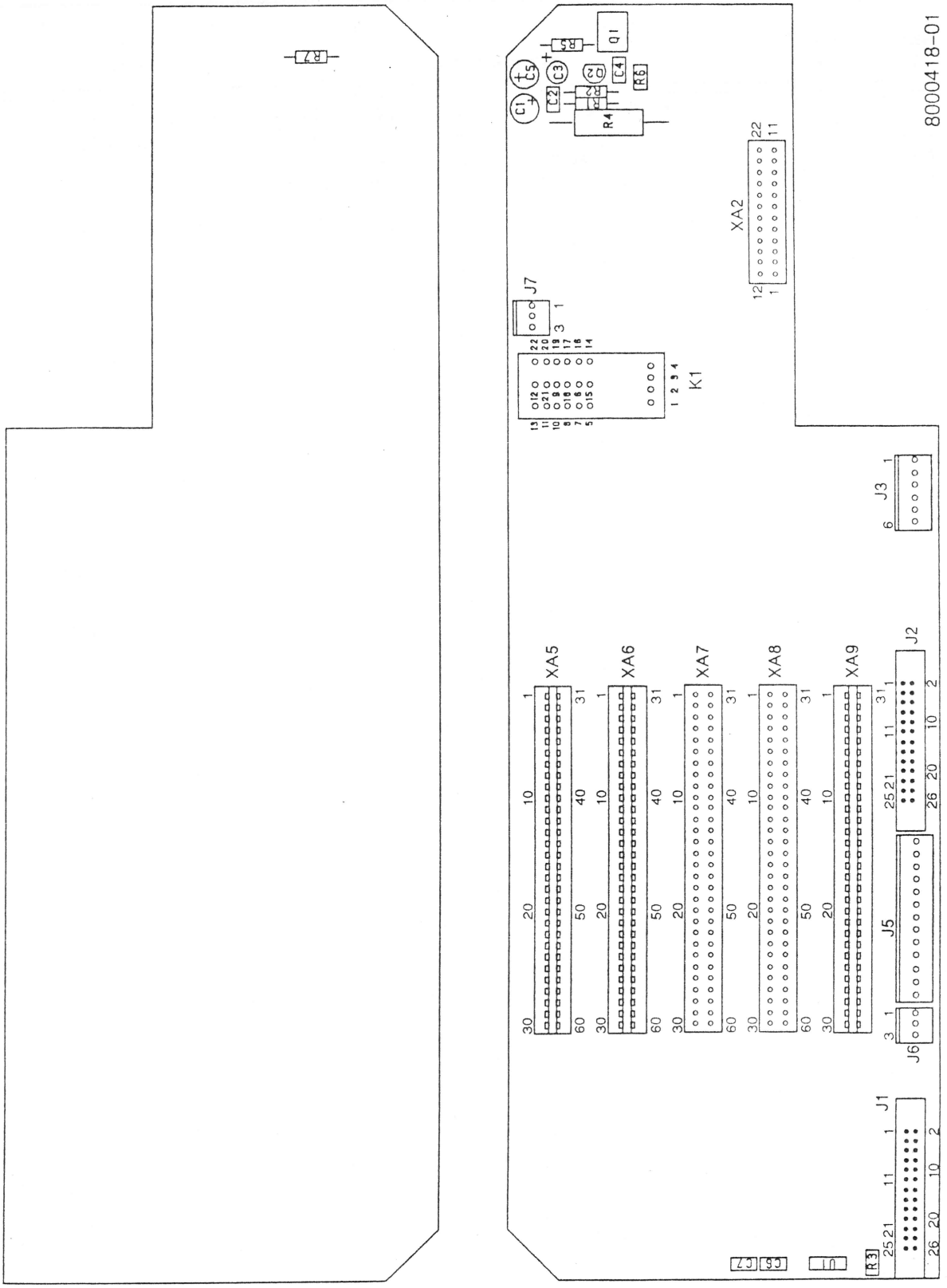
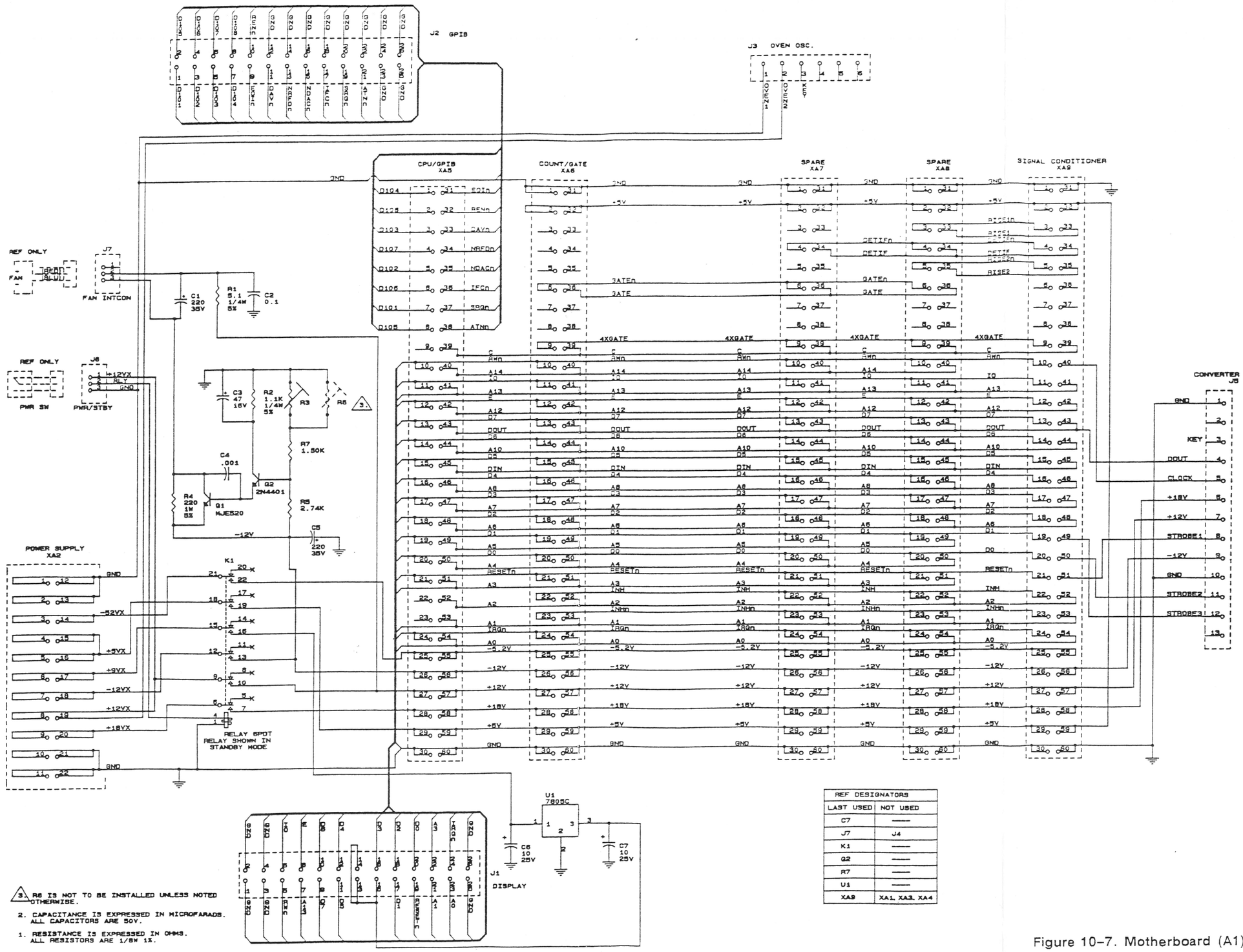



Figure 10-6. Motherboard (A1) Component Locator.




| REF DESIGNATORS | |
|---|---|
| LAST USED | NOT USED |
| C7 | —— |
| J7 | J4 |
| K1 | —— |
| Q2 | —— |
| R7 | —— |
| U1 | —— |
| XA9 | XA1, XA3, XA4 |

5500418-02

Figure 10-7. Motherboard (A1) Schematic Diagram

REV. 10/25/90

10-15/10-16

BACKDATE 5580076-00

## A2
## POWER SUPPLY
## (2020417-02)

The Power Supply assembly receives ac voltages of 16 Vrms and 30 Vrms from the secondary windings on the power transformer. These ac voltages are full wave rectified by CR1 and CR2 and provide two unregulated dc voltages: +9 and +18 V, and four regulated dc voltages: +5 V, -5.2 V, +12 V, and -12 V.

The positive rectified voltage from CR1 is filtered by C4 and used as the source for the +18 V unregulated supply. The +18 V unregulated supply is also fed to U2, a 12 V three terminal regulator. Variable resistor R3 provides adjustment for the +12 V supply.

The negative rectified voltage from CR1 is filtered by C5 and fed to U3, a -12 V three terminal regulator. Variable resistor R6 provides adjustment for the -12 V supply.

The positive rectified voltage from CR2 is filtered by C1 and used as the source for the +9 V unregulated supply. The +9 V unregulated supply is used to drive the front panel display. The +9 V unregulated supply is also fed to U1, a +5 V three terminal regulator. Jumpers W1 and W2 are provided for adjustment of the +5 V supply.

The negative rectified voltage from CR2 is filtered by C2 and fed to U4, a -5.2 V three terminal regulator. There is no adjustment provided for the -5.2 V supply.

Connector J3 provides an input for an external 12 V supply. This external supply connects to a rear panel connector and is used to power the optional oven oscillator during transit.

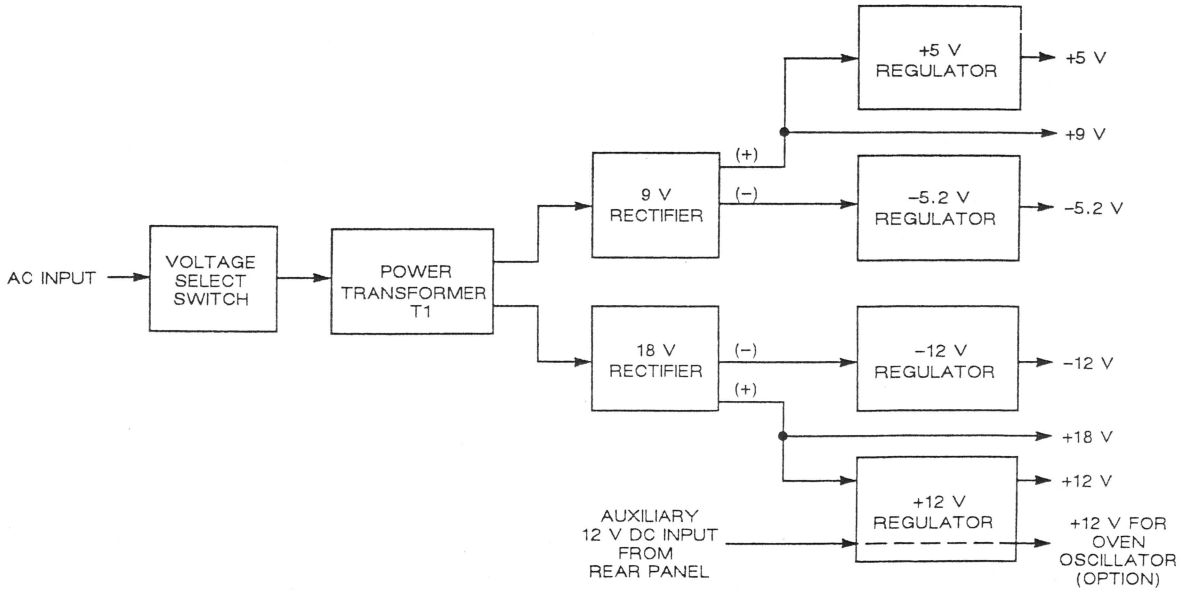



Figure 10-1. Power Supply Functional Block Diagram.

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## A2 POWER SUPPLY 2020417-02 Rev. A

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,ALUM ELCTLT | 33,000µF | | 16VDC | 2100130-00 | 2 |
| C2 | C1 | | | | | | |
| C3 | | CAP,TANTALUM | 10µF | 20% | 25V | 2300029-00 | 4 |
| C4 | | CAP,ALUM ELCTLT | 15,000µF | | 25VDC | 2100129-00 | 1 |
| C5 | | CAP,ALUM ELCTLT | 10,000µF | | 25VDC | 2100131-00 | 1 |
| C6 | C3 | | | | | | |
| C7 | | CAP,TANTALUM | 1µF | 20% | 35V | 2300008-00 | 3 |
| C8 | C3 | | | | | | |
| C9 | | NOT USED | | | | | |
| C10 | C3 | | | | | | |
| C11 | C7 | | | | | | |
| C12 | C7 | | | | | | |
| C13 | | CAP,ML CER | 1µF | 20% | 50V | 2150023-00 | 4 |
| C14 | C13 | | | | | | |
| C15 | C13 | | | | | | |
| C16 | C13 | | | | | | |
| C17 | | CAP,DISC,CER | .002µF | 20% | 1KV | 2150005-00 | 1 |
| CR1 | | DIODE,MDA970-2,BRIDGE,100V | | | | 2710045-00 | 1 |
| CR2 | | DIODE,MDA990-1,BRIDGE | | | | 2710028-00 | 1 |
| CR3 | | DIODE,1N4003,GP RECTIFIER | | | | 2700004-00 | 2 |
| CR4 | CR3 | | | | | | |
| CR5 | | DIODE,ZENER OVERVOLTAGE,SA16,16V | | | | 2700007-00 | 1 |
| J1 | | CONN,SQ POST,6 PIN,156 | | | | 2620157-00 | 1 |
| J2 | | CONN,SQ,POST,3 PIN,156 | | | | 2620154-00 | 1 |
| J3 | | CONN,POST,SQ 156,2 PIN | | | | 2620153-00 | 1 |
| L1 | | INDUCTOR,4700µH | | | | 3510017-00 | 1 |
| R1 | | RES,M/OX | 475 | 1/10W | 1% | 4054750-00 | 1 |
| R2 | | RES,M/OX | 3.01K | 1/8W | 1% | 4053011-00 | 1 |
| R3 | | POT,CERMET,TO5 | 2K . | 5W | 10% | 4250016-00 | 2 |
| R4 | | NOT USED | | | | | |
| R5 | | NOT USED | | | | | |
| R6 | R3 | | | | | | |
| R7 | | RES,M/OX | 8.66K | 1/8W | 1% | 4068661-00 | 1 |
| R8 | | RES,M/OX | 1.21K | 1/10W | 1% | 4051211-00 | 1 |
| R9 | | RES,M/OX | 200 | 1/4W | 2% | 4130201-00 | 1 |
| R10 | | RES,CC | 5.6 | 1/4W | 5% | 4010569-00 | 1 |
| R11 | | RES,M/OX | 13 | 1/4W | 2% | 4130130-00 | 1 |
| R12 | | RES,CC | 4.7 | 1/4W | 5% | 4010479-00 | 1 |
| TP1 | | CONN,PIN-TP,SWAGE .040D-.150L | | | | 2620193-00 | 4 |
| TP2 | TP1 | | | | | | |
| TP3 | TP1 | | | | | | |
| TP4 | TP1 | | | | | | |
| U1 | | IC,78H05A,VOLT RGLTR,+5V,TO-3 | | | | 3057805-01 | 1 |
| U2 | | IC,LM350T,3A,RGLTR,ADJ,POS,TO-220 | | | | 3040350-00 | 1 |
| U3 | | IC,LM337,VOLT RGLTR,ADJ,NEG,TO-220 | | | | 3040337-00 | 1 |
| U4 | | IC,LM345-5.2,VOLT RGLTR,NEG,TO-3 | | | | 3040345-00 | 1 |

## A2 POWER SUPPLY (Continued) 2020417-02 Rev. A

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| HARDWARE USED IN THIS ASSEMBLY | | | | |
| | | BRACKET,HEATSINK,P.S. | 5210860-02 | 1 |
| | | PAD,INSULATOR,SILICON TO-220 | 5000235-00 | 2 |
| | | INSULATOR,SILICON TO-3 | 5000239-00 | 2 |
| | | NUT,HEX,CRES 4-40 UNC-2B | 5180004-40 | 4 |
| | | BUSHING,NYLON INSUL | 5000159-00 | 2 |
| | | SCR,PNH X-REC 6-32X3/4 UNC | 5120006-12 | 1 |
| | | SCR,PNH X-REC 4-40X3/16 UNC | 5120004-03 | 2 |
| | | WASH,LK,INTL-T,CRES # 4 | 5163004-00 | 8 |
| | | WASHER,FLAT,CRES,REDUCED O.D. NO.4 | 5161004-00 | 2 |
| | | SCR,PNH X-REC 6-32X1/4 UNC | 5120006-04 | 2 |
| | | WASH,LK,INTL-T,CRES # 6 | 5163006-00 | 3 |
| | | WIRE,BUS,18AWG | 5460011-00 | 10 |
| | | TUBING,TEFLON 18 AWG CLR | 5480012-00 | 9 |
| | | SCR,PNH X-REC 4-40X3/8 UNC | 5120004-06 | 4 |
| | | PCB SCHEMATIC DIAGRAM | 5500417-02 A | REF. |

Power Supply Component Locator
(PCB Assembly A2)

(See following page)

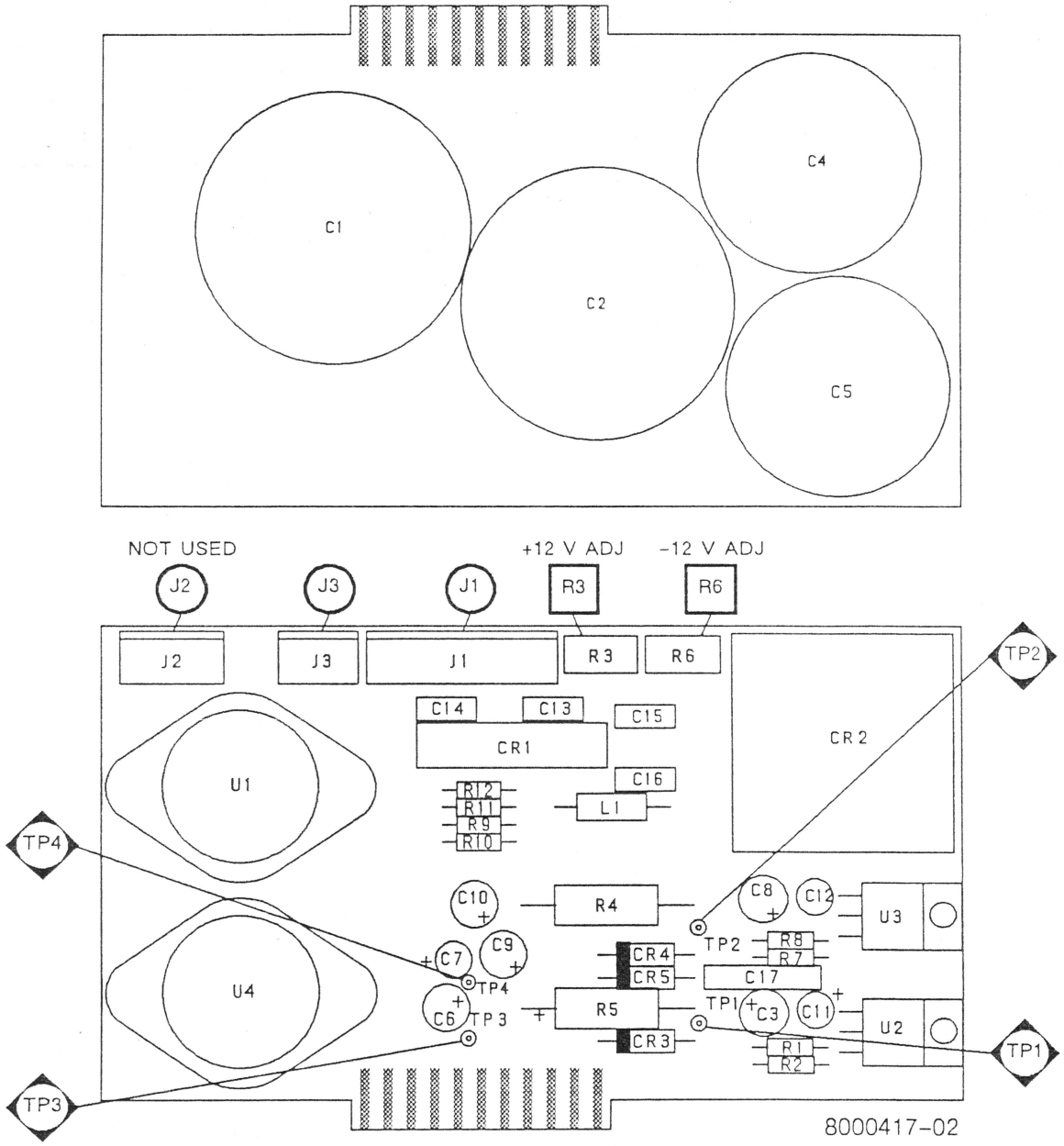
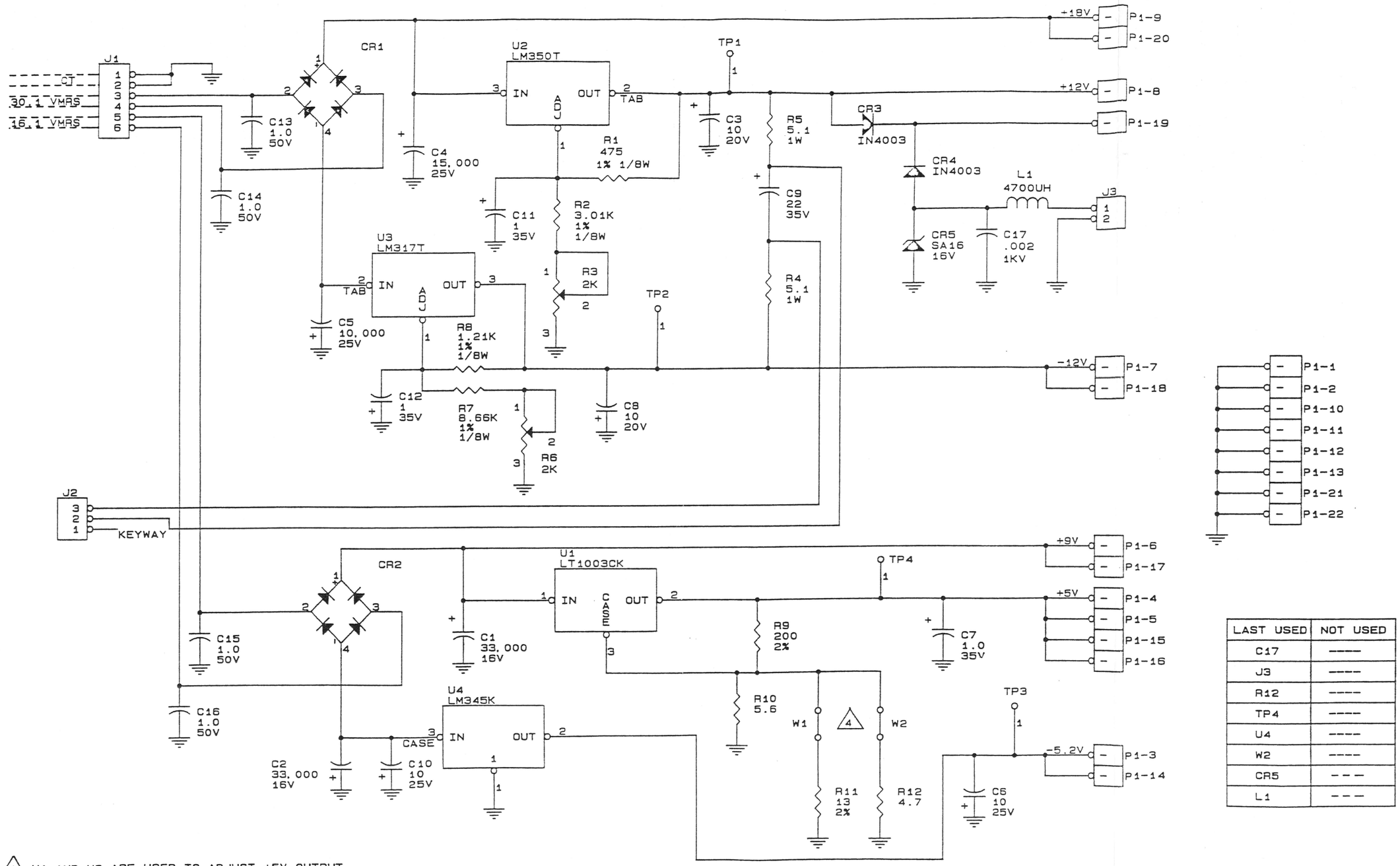



Figure 10-9. Power Supply (A2) Component Locator.




| LAST USED | NOT USED |
|---|---|
| C17 | ----- |
| J3 | ----- |
| R12 | ----- |
| TP4 | ----- |
| U4 | ----- |
| W2 | ----- |
| CR5 | - - - |
| L1 | - - - |

4. W1 AND W2 ARE USED TO ADJUST +5V OUTPUT. SEE TEST PROCEDURE FOR DETAILS.

3. PREFIX FOR ALL REF. DESIG: A2.

2. ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.

1. ALL FIXED RESISTORS ARE 1/4W +/-5%. ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

5500417-02

Figure 10-10. Power Supply (A2) Schematic Diagram

# A6
# COUNT CHAIN/GATE
# (2020421-01)

The Count Chain/Gate assembly consists of two functionally distinct circuits. The first is the gate generation circuitry which provides the precise gate time interval required for frequency measurements. The second is the count chain circuitry which counts the number of zero-crossings of the input signal occurring during the gate time interval.

## GATE CIRCUITRY

The gate circuitry consists of the following functional blocks:

- 10 MHz time base
- Internal/external time base select
- Time base divider
- Clock select
- Gate generator

### GENERAL DESCRIPTION

The internal 10 MHz time base signal, or alternatively the external time base signal, is selected by the time base select circuitry and used to provide an accurate time reference. This signal is used for gate generation and as the frequency reference for the phase-locked VCO (used as the local oscillator for downconversion). While using the internal time base, a sample of this signal is applied to the 10 MHz IN/OUT connector on the rear panel of the counter. This allows for the use of the internal time base as a system reference.

The 10 MHz signal used for gate generation is applied to a synchronous divide-by-100 circuit, consisting of U4 and U5, where it is divided down to a 100 kHz signal. To compensate for prescaling the Band 2 input signal by a factor of four, the gate time must be increased by the same factor. This is accomplished by again dividing the clock, by a factor of four, down to 25 kHz. The divided clock is applied to the gate generator circuit which, through microprocessor control, provides a gate signal with the precise time interval required by the count chain for frequency measurements.

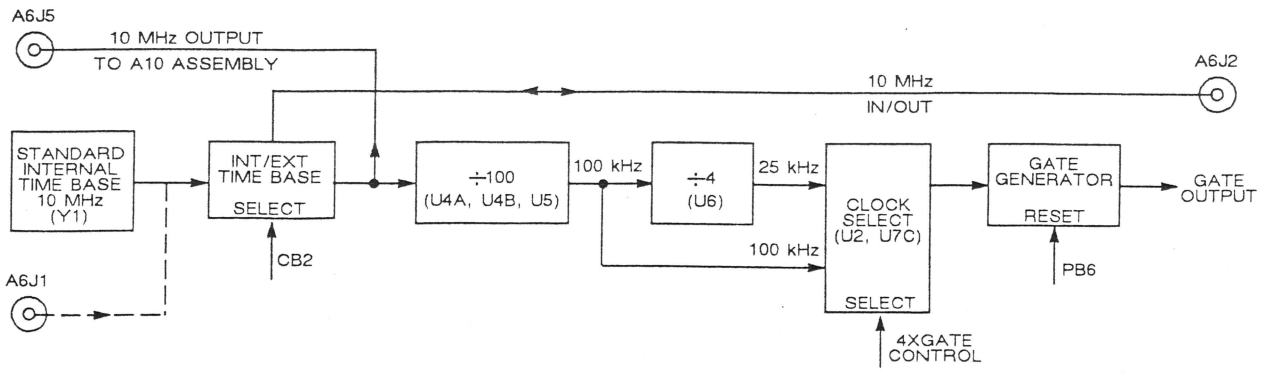



Figure 10-14. Gate Generation Functional Block Diagram.

## 10 MHz TIME BASE

The internal 10 MHz time base provides the time reference required for frequency measurements. The frequency accuracy of this signal determines how accurately the counter can perform frequency measurements. The standard time base used in the counter is a TCXO (Temperature Compensated Crystal Oscillator) which is physically mounted on this assembly, designated as Y1. An optional high stability ovenized time base is available for the counter which can improve the measurement accuracy of the instrument. On counters with this option, the standard TCXO is replaced by connector J1, which connects to the high stability time base.

## INTERNAL/EXTERNAL TIME BASE SELECT

The time base select circuitry allows the user to select between the internal time base and an external 10 MHz signal applied at the rear panel 10 MHz IN/OUT connector.

In the internal mode, the 10 MHz signal from the internal time base (Y1) is applied to buffer amplifier Q6. Q6 then amplifies the signal and provides the isolation necessary to maintain a constant load on the internal time base. In the internal mode, Q2 is turned off which allows Q5 to pass the signal from the emitter of Q6 to the base of Q7. Q7 serves as an emitter follower which drives the rear panel 10 MHz IN/OUT connector. The signal from the collector of Q6 is applied to pin 12 of U1D, a NAND gate which also serves as a Schmitt trigger, for sine wave to square wave conversion. When the internal time base is selected, the signal at U1A pin 2 is a TTL low causing the output from U1A pin 3 to be a TTL high. The TTL high from U1A pin 3 is applied to U1D pin 13 causing the 10 MHz signal on U1D pin 12 to be passed through to U1C pin 9. In the internal mode, the signal on U1C pin 10 is a TTL high causing the 10 MHz signal on U1C pin 9 to be passed through to U1C pin 8, the output of the time base select circuit.

In the external mode, a 10 MHz external time base signal from the rear panel 10 MHz IN/OUT connector is applied through C3 and R10 to the base of emitter-follower Q3. In the external mode Q1 is turned off which allows Q4 to pass the external 10 MHz signal from the emitter of Q3 to U1B pin 4, a NAND gate which also serves as a Schmitt trigger. Selecting the external time base mode causes the microprocessor to set U1B pin 5 (CB2) high causing the 10 MHz signal on U1B pin 4 to be passed through to U1C pin 10. In the external mode, the signal on U1C pin 9 is a TTL high. This causes the 10 MHz signal on U1C pin 10 to be passed through to U1C pin 8, the output of the time base select circuit.

The 10 MHz output from the time base select circuitry follows two paths. One path is through U2D, a 50 ohm inverting buffer/driver. The signal output at U2D pin 11 is fed to a low pass filter, consisting of L1, C9, and C12. This filter converts the signal back to a sine wave by reducing its harmonic content. The 10 MHz sine wave from J5 is routed to the microwave converter, where it serves as the frequency reference for the phase-locked VCO. The second path out of the time base select circuitry feeds the signal to the divider/gate generation circuitry.

## TIME BASE DIVIDER

The divider circuit receives the 10 MHz square wave reference from the time base select circuitry and synchronously divides it down into two clock signals: a 100 kHz signal and a 25 kHz signal. By synchronously dividing the input, transitions in both the 100 kHz and 25 kHz clock signals occur only during transitions of the 10 MHz reference signal. The 100 kHz signal is obtained by dividing the input signal by a factor of 100 in U4A, U4B, and U5. The 25 kHz signal is obtained by dividing the 100 kHz signal by a factor of 4 using U6, which consists of two D-type flip-flops.

## A6 COUNT CHAIN/GATE 2020421-01 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|
| C1 | | CAP,ML CER | .01µF | 10% 100V | 2150014-00 | 36 |
| C2 | C1 | | | | | |
| C3 | C1 | | | | | |
| C4 | C1 | | | | | |
| C5 | C1 | | | | | |
| C6 | C1 | | | | | |
| C7 | C1 | | | | | |
| C8 | C1 | | | | | |
| C9 | C1 | | | | | |
| C10 | C1 | | | | | |
| C11 | C1 | | | | | |
| C12 | C1 | | | | | |
| C13 | C1 | | | | | |
| C14 | C1 | | | | | |
| C15 | C1 | | | | | |
| C16 | C1 | | | | | |
| C17 | | CAP,DISC,CER | .1µF | 50V | 2150092-00 | 1 |
| C18 | | CAP,ML,NPO | 1000PF | 5% 50V | 2350046-00 | 6 |
| C19 | C18 | | | | | |
| C20 | C1 | | | | | |
| C21 | C18 | | | | | |
| C22 | | CAP,ML,NPO | 390PF | 5% 50V | 2350047-00 | 1 |
| C23 | | CAP,TANTALUM | 33µF | 20% 10V | 2300015-00 | 3 |
| C24 | C23 | | | | | |
| C25 | C23 | | | | | |
| C26 | | CAP,TANTALUM | 10µF | 20% 25V | 2300029-00 | 4 |
| C27 | C26 | | | | | |
| C28 | C26 | | | | | |
| C29 | C26 | | | | | |
| C30 | | CAP,TANTALUM | 100µF | 20% 6.3V | 2300024-00 | 1 |
| C31 | | CAP,MICA | 15PF | 5% 500V | 2260014-00 | 1 |
| C32 | | CAP,CER | 220PF | 10% 100V | 2150047-00 | 1 |
| C33 | C1 | | | | | |
| C34 | C1 | | | | | |
| C35 | C1 | | | | | |
| C36 | C1 | | | | | |
| C37 | C1 | | | | | |
| C38 | C1 | | | | | |
| C39 | C1 | | | | | |
| C40 | C1 | | | | | |
| C41 | C1 | | | | | |
| C42 | C1 | | | | | |
| C43 | C1 | | | | | |
| C44 | C1 | | | | | |
| C45 | C1 | | | | | |
| C46 | C1 | | | | | |
| C47 | C1 | | | | | |
| C48 | C1 | | | | | |
| C49 | C1 | | | | | |
| C50 | C1 | | | | | |
| C51 | C18 | | | | | |
| C52 | C1 | | | | | |
| C53 | C18 | | | | | |
| C54 | C18 | | | | | |
| CR1 | | DIODE,1N5234,ZENER 6.2V | | | 2705234-00 | 1 |
| J1 | | CONN,COAX PC RCPT,SNAP NANOHEX | | | 2610038-00 | 5 |
| J2 | J1 | | | | | |
| J3 | J1 | | | | | |
| J4 | J1 | | | | | |
| J5 | J1 | | | | | |

## A6 COUNT CHAIN/GATE (Continued) 2020421-01 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| L1 | | INDUCTOR,1.0µH | | | | 3510003-00 | 1 |
| L2 | | INDUCTOR,.068µH,REF CHK | | | | 3520017-00 | 1 |
| L3 | | INDUCTOR,5.6µH | | | | 3510036-00 | 1 |
| Q1 | | XSTR,2N4124,NPN,GP | | | | 4704124-00 | 4 |
| Q2 | Q1 | | | | | | |
| Q3 | Q1 | | | | | | |
| Q4 | Q1 | | | | | | |
| Q5 | | XSTR,2N4126,PNP,GP | | | | 4704126-00 | 3 |
| Q6 | Q5 | | | | | | |
| Q7 | Q5 | | | | | | |
| Q8 | | XSTR,NE02137,NPN,MICROWAVE | | | | 4710032-00 | 4 |
| Q9 | Q8 | | | | | | |
| Q10 | Q8 | | | | | | |
| Q11 | Q8 | | | | | | |
| Q12 | | XSTR,MRF536,PNP,RF | | | | 4710044-00 | 2 |
| Q13 | Q12 | | | | | | |
| Q14 | | XSTR,MMBT3960,NPN SWITCHING | | | | 1410101-00 | 1 |
| R1 | | RES,M/OX | 332 | 1/8W | 1% | 4063320-00 | 4 |
| R2 | R1 | | | | | | |
| R3 | R1 | | | | | | |
| R4 | R1 | | | | | | |
| R5 | | RES,M/OX | 1K | 1/8W | 1% | 4061001-00 | 12 |
| R6 | R5 | | | | | | |
| R7 | R5 | | | | | | |
| R8 | R5 | | | | | | |
| R9 | R5 | | | | | | |
| R10 | R5 | | | | | | |
| R11 | | RES,M/OX | 301 | 1/8W | 1% | 4063010-00 | 1 |
| R12 | R5 | | | | | | |
| R13 | | RES,M/OX | 511 | 1/8W | 1% | 4065110-00 | 3 |
| R14 | R13 | | | | | | |
| R15 | R13 | | | | | | |
| R16 | | RES,M/OX | 2.00K | 1/8W | 1% | 4062001-00 | 2 |
| R17 | R16 | | | | | | |
| R18 | | RES,M/OX | 1.82K | 1/8W | 1% | 4061821-00 | 1 |
| R19 | | RES,M/OX | 39.2 | 1/8W | 1% | 4063929-00 | 3 |
| R20 | | RES,M/OX | 619 | 1/10W | 1% | 4056190-00 | 2 |
| R21 | | RES,M/OX | 2.21K | 1/8W | 1% | 4062211-00 | 3 |
| R22 | | RES,M/OX | 200 | 1/8W | 1% | 4062000-00 | 1 |
| R23 | | RES,M/OX | 10.0 | 1/8W | 1% | .4061009-00 | 3 |
| R24 | | RES,M/OX | 221 | 1/10W | 1% | 4052210-00 | 2 |
| R25 | R23 | | | | | | |
| R26 | R20 | | | | | | |
| R27 | R24 | | | | | | |
| R28 | R21 | | | | | | |
| R29 | | RES,M/OX | 27.4 | 1/8W | 1% | 4062749-00 | 1 |
| R30 | | RES,M/OX | 4.75K | 1/8W | 1% | 4064751-00 | 4 |
| R31 | R30 | | | | | | |
| R32 | R30 | | | | | | |
| R33 | R30 | | | | | | |
| R34 | R21 | | | | | | |
| R35 | | RES,M/OX | 2.74K | 1/10W | 1% | 4052741-00 | 1 |
| R36 | | RES,M/OX | 51.1 | 1/8W | 1% | 4065119-00 | 2 |
| R37 | | RES,M/OX | 100 | 1/8W | 1% | 4061000-00 | 1 |
| R38 | | RES,M/OX | 274 | 1/8W | 1% | 4062740-00 | 1 |
| R39 | R36 | | | | | | |
| R40 | | RES,M/OX | 130.0 | 1/8W | 1% | 4061300-00 | 2 |
| R41 | | RES,M/OX | 82.5 | 1/8W | 1% | 4068259-00 | 2 |
| R42 | R40 | | | | | | |

## A6 COUNT CHAIN/GATE (Continued) 2020421-01 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| R43 | R41 | | | | | | |
| R44 | | RES,CC | 5.6 | 1/4W | 5% | 4010569-00 | 3 |
| R45 | R44 | | | | | | |
| R46 | R44 | | | | | | |
| R47 | | RES,M/OX | 56.2 | 1/8W | 1% | 4065629-00 | 2 |
| R48 | R47 | | | | | | |
| R49 | | RES,M/OX | 487 | 1/10W | 1% | 4054870-00 | 2 |
| R50 | | RES,SMD | 47.5 | 1/8W | 1% | 4234759-00 | 1 |
| R51 | R19 | | | | | | |
| R52 | R19 | | | | | | |
| R53 | R23 | | | | | | |
| R54 | R5 | | | | | | |
| R55 | | RES,M/OX | 20.0K | 1/8W | 1% | 4062002-00 | 4 |
| R56 | R55 | | | | | | |
| R57 | R55 | | | | | | |
| R58 | R55 | | | | | | |
| R59 | | RES,M/OX | 10.0K | 1/8W | 1% | 4061002-00 | 7 |
| R60 | R59 | | | | | | |
| R61 | R59 | | | | | | |
| R62 | R59 | | | | | | |
| R63 | | RES,M/OX | 750K | 1/4W | 2% | 4130754-00 | 1 |
| R64 | | RES,M/OX | 90.9 | 1/8W | 1% | 4069099-00 | 1 |
| R65 | R49 | | | | | | |
| R66 | R59 | | | | | | |
| R67 | R59 | | | | | | |
| R68 | R59 | | | | | | |
| R69 | R5 | | | | | | |
| R70 | R5 | | | | | | |
| R71 | | RES,M/OX | 3.01K | 1/8W | 1% | 4063011-00 | 1 |
| R72 | R5 | | | | | | |
| R73 | R5 | | | | | | |
| TP1 | | CONN,PCB,.040D PIN,GOLD | | | | 2620032-00 | 10 |
| TP2 | TP1 | | | | | | |
| TP3 | TP1 | | | | | | |
| TP4 | TP1 | | | | | | |
| TP5 | TP1 | | | | | | |
| TP6 | TP1 | | | | | | |
| TP7 | TP1 | | | | | | |
| TP8 | TP1 | | | | | | |
| TP9 | TP1 | | | | | | |
| TP10 | TP1 | | | | | | |
| U1 | | IC,10125,ECL 10K,TRANSLATORS | | | | 3110125-00 | 1 |
| U2 | | IC,74LS490 | | | | 3084490-00 | 1 |
| U3 | | IC,MC10131L,DUAL,M-S FF | | | | 3110131-00 | 1 |
| U4 | | IC,74ACT00PC | | | | 3110011-00 | 1 |
| U5 | | IC,74LS132 | | | | 3084132-00 | 1 |
| U6 | | IC,10H116,ECL 10KH,LINE RCVRS | | | | 3118116-00 | 1 |
| U7 | | IC,LM741C,OP AMP | | | | 3040741-00 | 1 |
| U8 | | IC,SP8637B,HIGH SPEED DIVIDERS/10 | | | | 3010637-00 | 1 |
| U9 | | IC,74LS196 | | | | 3084196-00 | 1 |
| U10 | | IC,74LS160 | | | | 3084160-00 | 1 |
| U11 | | IC,LS7031,CNTR,6-DECADE,UP,PMDS | | | | 3057031-00 | 1 |
| U12 | | IC,74LS04 | | | | 3087404-00 | 1 |
| U13 | | IC,74LS175 | | | | 3084175-00 | 1 |
| U14 | | IC,MK5009N,P-CHANNEL MOS DIVIDER | | | | 3035009-00 | 1 |
| U15 | | IC,74LS74 | | | | 3087474-00 | 2 |
| U16 | | IC,74LS02 | | | | 3087402-00 | 1 |
| U17 | | IC,555,TIMER | | | | 3040555-00 | 1 |
| U18 | | IC,MC68B21P,PRPHL INTERFACE ADAPTER | | | | 3086821-00 | 1 |
| U19 | U15 | | | | | | |

## A6 COUNT CHAIN/GATE (Continued) 2020421-01 Rev. D

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| XU1 | | NOT USED | | |
| XU2 | | NOT USED | | |
| XU3 | | NOT USED | | |
| XU4 | | NOT USED | | |
| XU5 | | NOT USED | | |
| XU6 | | NOT USED | | |
| XU7 | | NOT USED | | |
| XU8 | | NOT USED | | |
| XU9 | | NOT USED | | |
| XU10 | | NOT USED | | |
| XU11 | | CONN,SOCKET,DIP,40 PIN | 2630022-00 | 2 |
| XU12 | | NOT USED | | |
| XU13 | | NOT USED | | |
| XU14 | | NOT USED | | |
| XU15 | | NOT USED | | |
| XU16 | | NOT USED | | |
| XU17 | | NOT USED | | |
| XU18 | XU11 | CONN,SOCKET,DIP,40 PIN | 2630022-00 | 2 |
| XU19 | | NOT USED | | |
| Y1 | OSC,TCXO | 2030002-00 | 1 | |

HARDWARE USED IN THIS ASSEMBLY

| | | | |
|---|---|---|---|
| | HANDLE,PCB | 5230001-00 | 2 |
| | PIN,ROLL,3/32 DIA 1/4 LG | 5110008-00 | 2 |
| | TAPE,DBL SIDED,TFR 3/4IN | 5601006-00 | 1 |
| | WIRE,INSUL,30AWG,GREEN | 5430555-00 | 15 |
| | TUBING,SHRINK,3/64 CLEAR | 5480001-00 | 2 |
| | PCB SCHEMATIC DIAGRAM | 5500421-01 B | REF. |

Count Chain/Gate Component Locator
(PCB Assembly A6)

(See following page)

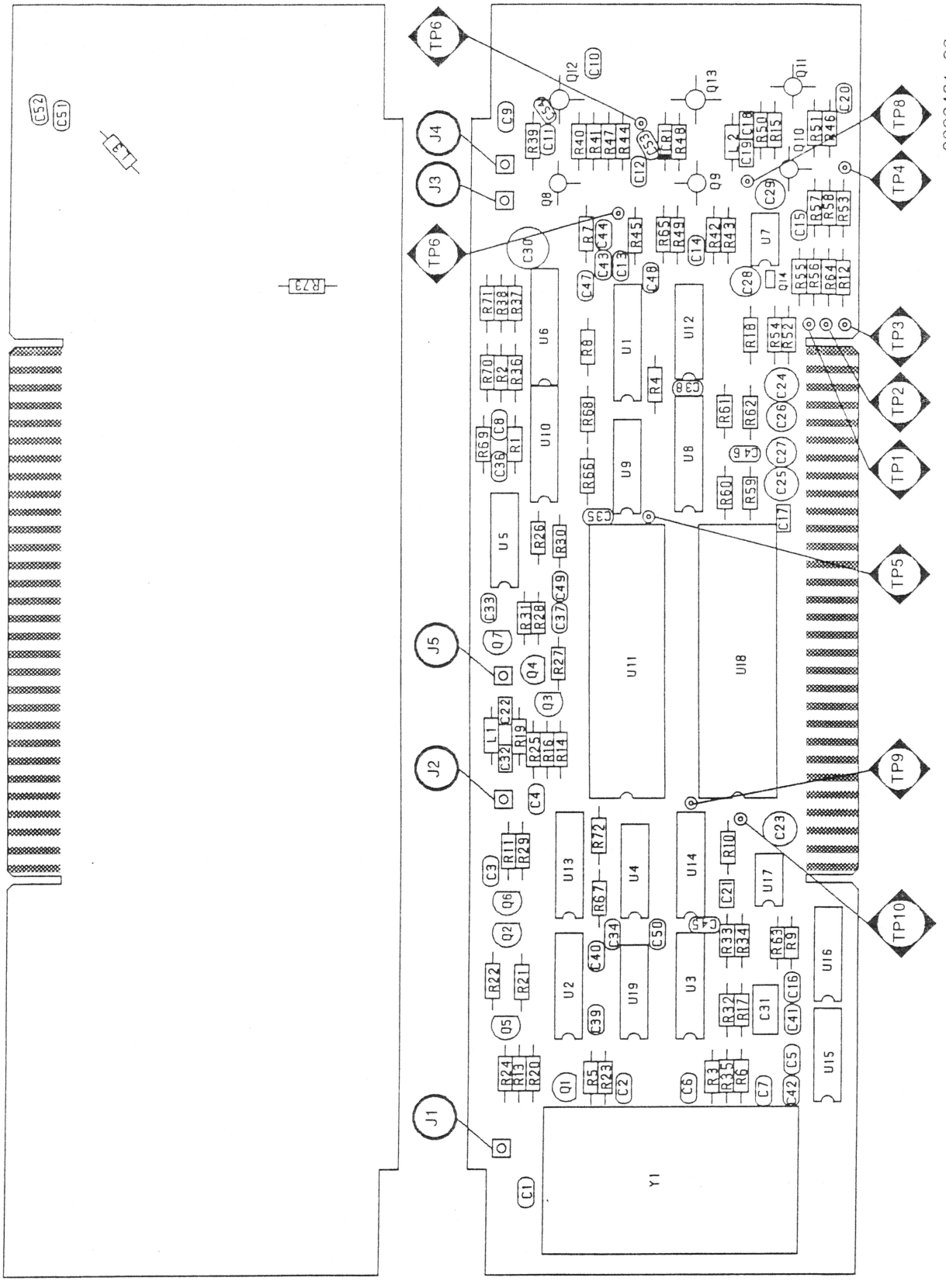
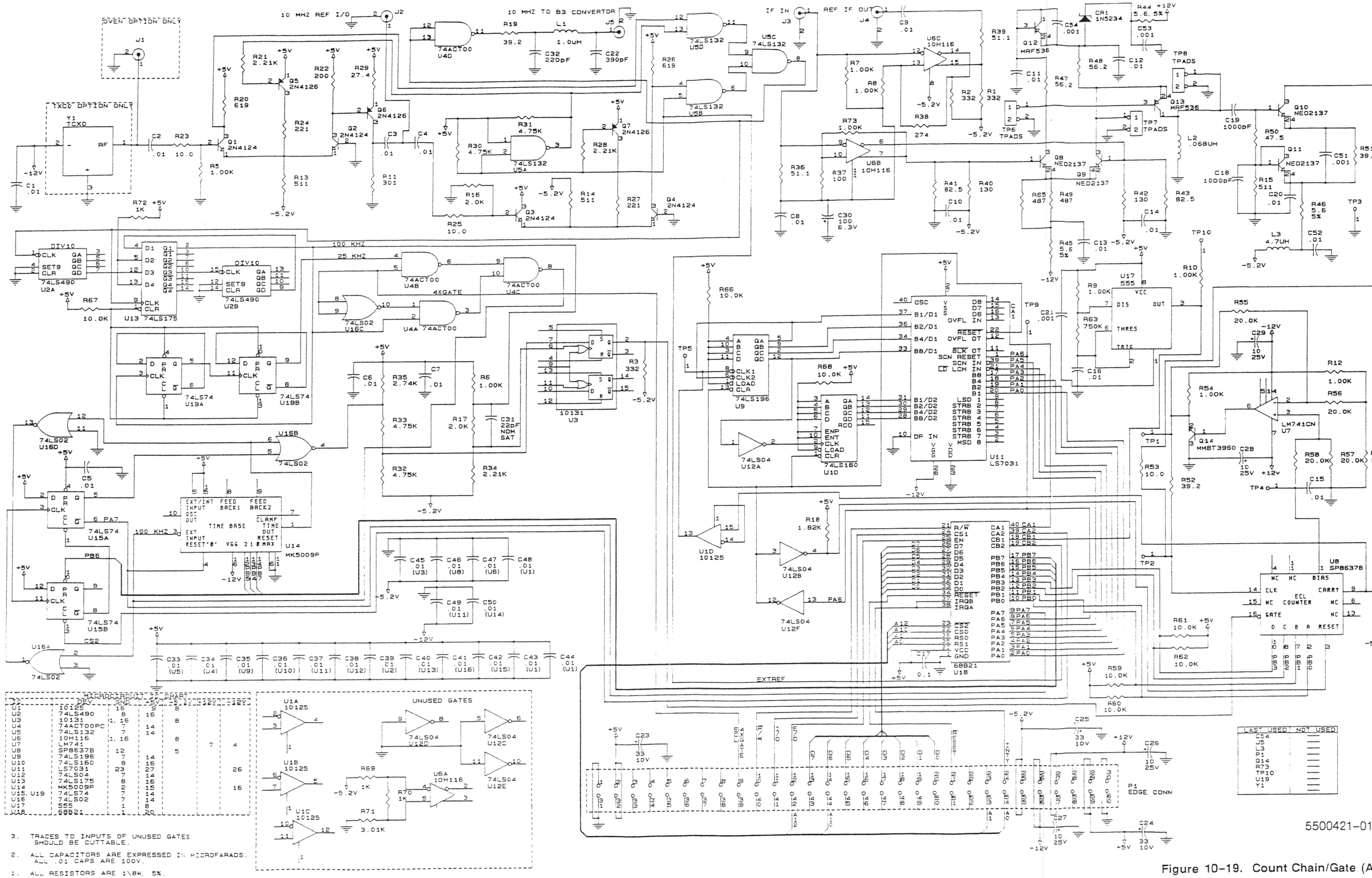



Figure 10-18. Count Chain/Gate (A6) Component Locator.




| IC | DEV | GND | +5V | -5.2V | +12V | -12V |
|---|---|---|---|---|---|---|
| U1 | 10125 | 16 | 8 | | | |
| U2 | 74LS490 | 8 | 16 | | | |
| U3 | 10131 | 1, 16 | 8 | | | |
| U4 | 74ACT00PC | 7 | 14 | | | |
| U5 | 74LS132 | 7 | 14 | | | |
| U6 | 10H116 | 1, 16 | 8 | | | |
| U7 | LM741 | | | 7 | 4 | |
| U8 | SPB637B | 12 | 5 | | | |
| U9 | 74LS196 | 7 | 14 | | | |
| U10 | 74LS160 | 8 | 16 | | | |
| U11 | LS7031 | 23 | 27 | | | 26 |
| U12 | 74LS04 | 7 | 14 | | | |
| U13 | 74LS175 | 8 | 16 | | | |
| U14 | MK5009P | 2 | 15 | | | 16 |
| U15, U19 | 74LS74 | 7 | 14 | | | |
| U16 | 74LS02 | 7 | 14 | | | |
| U17 | 555 | 1 | 8 | | | |
| U18 | 68B21 | 1 | 20 | | | |

3. TRACES TO INPUTS OF UNUSED GATES SHOULD BE CUTTABLE.
2. ALL CAPACITORS ARE EXPRESSED IN MICROFARADS. ALL .01 CAPS ARE 100V.
1. ALL RESISTORS ARE 1\8W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500421-01

Figure 10-19. Count Chain/Gate (A
Schematic Diagram.

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# A9
# SIGNAL CONDITIONER
# (2020420-02)

The Signal Conditioner assembly processes signals from all three bands, along with the self-test signal, and converts the selected signal into an ECL signal before being applied to the Count Chain/Gate generator assembly (A6) to be counted. Since the exact function varies depending on the input selected, a functional description for self-test and each of the various bands is provided.

## SELF-TEST

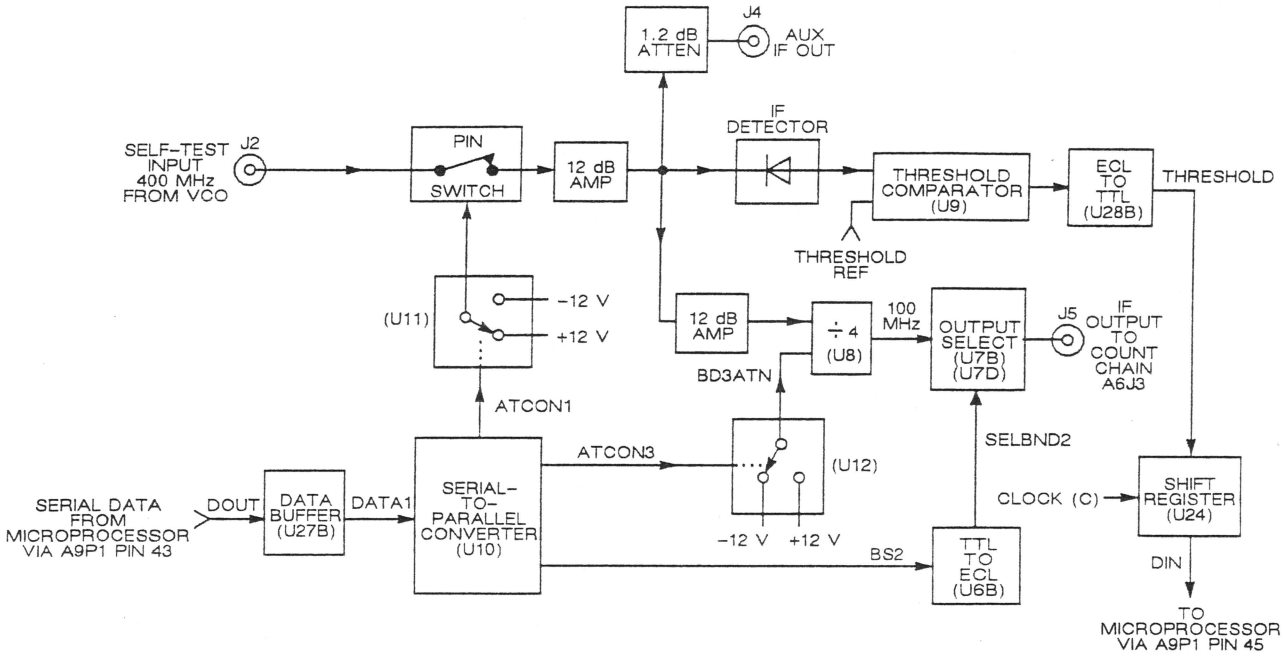



**Figure 10-20. Signal Conditioner Functional Block Diagram for Self-Test Mode.**

In the self-test mode, the input at J2 is a 400 MHz sine wave, at approximately -10 dBm, generated by the phase-locked VCO in the A10 assembly. This signal is passed through the PIN switch (CR4 and CR5) and amplifiers U5 and U4, to the divide-by-four IC, U8. The output of U8, 100 MHz in self-test, is gated through U7B and U7D to J5, the IF output to the A6 Count Chain/Gate assembly.

When the self-test mode is initiated, the microprocessor goes through a series of steps. The first step is to set the phase-locked VCO to 400 MHz. Next, the microprocessor sends, in the form of serial data, the commands necessary to set up the Signal Conditioner for the self-test mode.

The serial data is received at A9 on pin 43 of the edge connector (P1) as DOUT. The data passes through the constantly enabled line buffer (U27B) where the signal becomes DATA1. This signal (DATA1) is then routed to U10 pin 14 where it is converted from serial data to parallel data. The serial clock on U10 pin 11 (C), clocks the data in and the signal at pin 12 (STRB4) loads the output latches with the parallel data. The parallel data is applied to the TTL to ECL translators U6A through U6D and to analog switches U11 and U12. In the self-test mode, U10 pins 2 and 4 are TTL high and the remaining outputs are low.

The high output from U10 pin 4 is connected to the analog switch U11 at pin 15 closing the switch between pins 1 and 16, and opening the switch between pins 3 and 4. This causes the output on U11 pins 1 and 3 to be +12 Vdc causing the signal from J2 to pass through the pin switch, consisting of diodes CR4 and CR5.

The low output from U10 pin 6 is connected to the analog switch U12 at pin 15 opening the switch between pins 1 and 16, and closing the switch between pins 3 and 4. This causes the output on U12 pins 1 and 3 to be -12 Vdc. The -12 Vdc enables U8, the divide-by-four.

The high output from U10 pin 2 is passed through the TTL to ECL translator (U6B) to U7B pin 9. This enables the 100 MHz signal at U7B pin 8 to pass though U7B, through U7D and out J5, to the IF input on A6, the Count Chain/Gate generator assembly.

## BAND 1

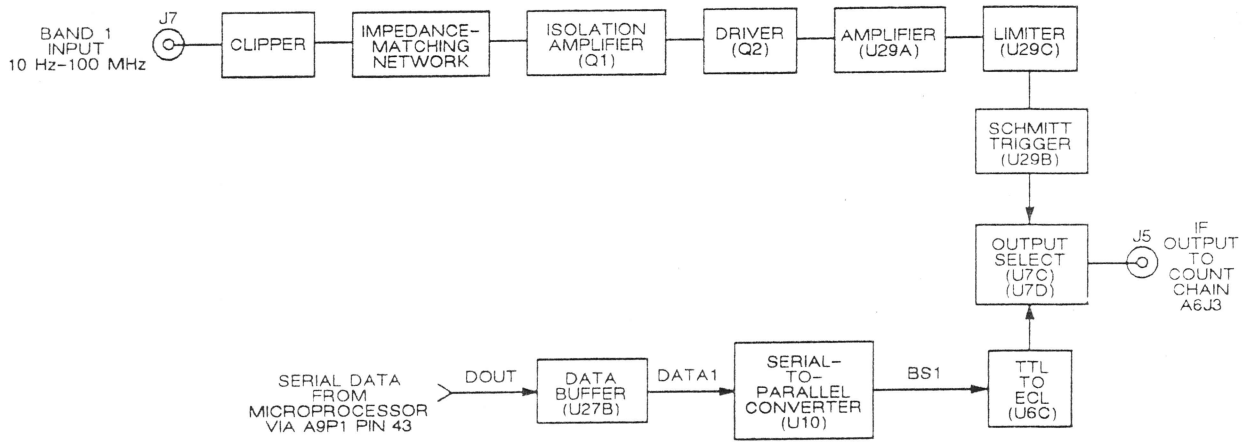



**Figure 10-21. Signal Conditioner Functional Block Diagram for Band 1.**

During Band 1 operation the Signal Conditioner converts the Band 1 input signal at J7 into an ECL signal and routes it to J5, the IF output to the A6 Count Chain assembly. The IF threshold circuit is disabled in this band and the counter continuously generates the gate signals for the count chain.

The Band 1 input signal (10 Hz to 100 MHz) from the front panel is directly connected to J7 on the Signal Conditioner. The amplitude of the input signal is limited to ±0.7 volts by CR15 and CR16. The impedance matching network in conjunction with Q1, the FET isolation amplifier, provides the 1 megohm input impedance. The signal from the source of Q1 is fed to Q2, a driver/current amplifier. The output from Q2 is ac coupled to amplifier U29A which is primarily used to amplify the lower level signals. The output of U29A is fed to the limiter U29C. The combination of U29A and U29C flattens the peaks of the input signal, providing a nearly constant amplitude output over the dynamic range of Band 1, at the input to U29B. The positive feedback on U29B, by R107, reduces the rise and fall time of the input signal from U29C, providing a sharp-edged square wave at U29B pin 9. The sharp edges on the output signal, at TP14, minimize the potential of false triggering due to noise.

When Band 1 is selected, the microprocessor sends, in the form of serial data, the commands necessary to set up the Signal Conditioner for Band 1 operation. The serial data is received at P1 pin 43 as DOUT. The data passes through the constantly enabled line buffer (U27B), where the signal becomes DATA1. This signal (DATA1) is then routed to U10 pin 14 where it is converted from serial

## A9 SIGNAL CONDITIONER 2020420-02 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C1 | | CAP,SMD,Z5U | .1µF | 20% | 50V | 2100046-00 | 58 |
| C2 | | CAP,SMD,CER,NPO | 100PF | 5% | 50V | 2100054-00 | 2 |
| C3 | C2 | | | | | | |
| C4 | | CAP,SMD,CER,NPO | 15PF | 5% | 50V | 2100072-00 | 1 |
| C5 | C1 | | | | | | |
| C6 | C1 | | | | | | |
| C7 | | CAP,SMD,CER,X7R | .001µF | 5% | 50V | 2100037-00 | 17 |
| C8 | C7 | | | | | | |
| C9 | C1 | | | | | | |
| C10 | C7 | | | | | | |
| C11 | C1 | | | | | | |
| C12 | C1 | | | | | | |
| C13 | C1 | | | | | | |
| C14 | C7 | | | | | | |
| C15 | C1 | | | | | | |
| C16 | C7 | | | | | | |
| C17 | C7 | | | | | | |
| C18 | C7 | | | | | | |
| C19 | C7 | | | | | | |
| C20 | C1 | | | | | | |
| C21 | C7 | | | | | | |
| C22 | C7 | | | | | | |
| C23 | C7 | | | | | | |
| C24 | C1 | | | | | | |
| C25 | C1 | | | | | | |
| C26 | C1 | | | | | | |
| C27 | C7 | | | | | | |
| C28 | C7 | | | | | | |
| C29 | C1 | | | | | | |
| C30 | C1 | | | | | | |
| C31 | C7 | | | | | | |
| C32 | C1 | | | | | | |
| C33 | C1 | | | | | | |
| C34 | C1 | | | | | | |
| C35 | C1 | | | | | | |
| C36 | C1 | | | | | | |
| C37 | C1 | | | | | | |
| C38 | C1 | | | | | | |
| C39 | C1 | | | | | | |
| C40 | C1 | | | | | | |
| C41 | C1 | | | | | | |
| C42 | C1 | | | | | | |
| C43 | C1 | | | | | | |
| C44 | | CAP,SMD,TANT | 47µF | 20% | 6V | 2100113-00 | 2 |
| C45 | C1 | | | | | | |
| C46 | C1 | | | | | | |
| C47 | C1 | | | | | | |
| C48 | C1 | | | | | | |
| C49 | C1 | | | | | | |
| C50 | C1 | | | | | | |
| C51 | | CAP,SMD,CER,X7R | .047µF | 10% | 50V | 2100044-00 | 1 |
| C52 | C1 | | | | | | |
| C53 | C1 | | | | | | |
| C54 | C7 | | | | | | |
| C55 | | CAP,SMD,CER,X7R | .033µF | 10% | 50V | 2100093-00 | 2 |
| C56 | C1 | | | | | | |
| C57 | C1 | | | | | | |
| C58 | C7 | | | | | | |
| C59 | C7 | | | | | | |
| C60 | C1 | | | | | | |
| C61 | C55 | | | | | | |
| C62 | C1 | | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-02 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| C63 | C1 | | | | | | |
| C64 | C1 | | | | | | |
| C65 | C1 | | | | | | |
| C66 | C1 | | | | | | |
| C67 | C1 | | | | | | |
| C68 | C1 | | | | | | |
| C69 | C1 | | | | | | |
| C70 | C1 | | | | | | |
| C71 | C44 | | | | | | |
| C72 | | CAP,SMD,TANT | 10µF | 10% | 25V | 2100043-00 | 2 |
| C73 | C72 | | | | | | |
| C74 | C1 | | | | | | |
| C75 | C1 | | | | | | |
| C76 | C1 | | | | | | |
| C77 | C1 | | | | | | |
| C78 | C1 | | | | | | |
| C79 | | CAP,SMD,CER,NPO | 82PF | 5% | 50V | 2100078-00 | 1 |
| C80 | | CAP,SMD,Z5U | 1µF | 20% | 50V | 2100108-00 | 1 |
| C81 | | CAP,SMD,CER,NPO | 8.2PF | | 50V | 2100061-00 | 1 |
| C82 | C1 | | | | | | |
| C83 | C1 | | | | | | |
| C84 | C1 | | | | | | |
| C85 | C1 | | | | | | |
| C86 | | CAP,TANTALUM | 100µF | 20% | 10V | 2300039-00 | 1 |
| C87 | C1 | | | | | | |
| C88 | | CAP,SMD,CER,NPO | 270PF | 5% | 50V | 2100079-00 | 1 |
| C89 | C1 | | | | | | |
| C90 | C1 | | | | | | |
| C91 | | CAP,ML CER | .001µF | 10% | 100V | 2150015-00 | 2 |
| C92 | C91 | | | | | | |
| CR1 | | DIODE,SMD,HSMP-3830,PIN | | | | 2700005-00 | 11 |
| CR2 | CR1 | | | | | | |
| CR3 | CR1 | | | | | | |
| CR4 | CR1 | | | | | | |
| CR5 | CR1 | | | | | | |
| CR6 | CR1 | | | | | | |
| CR7 | CR1 | | | | | | |
| CR8 | CR1 | | | | | | |
| CR9 | CR1 | | | | | | |
| CR10 | | DIODE,SMD,HSMS-2820,SCHOTTKY BARR | | | | 2740011-00 | 1 |
| CR11 | CR1 | | | | | | |
| CR12 | CR1 | | | | | | |
| CR13 | | DIODE,SMD,MMBD7000 | | | | 2740010-00 | 1 |
| CR14 | | NOT USED | | | | | |
| CR15 | | DIODE,1N914 | | | | 2700914-00 | 2 |
| CR16 | CR15 | | | | | | |
| J1 | | CONN,COAX PC RCPT,SNAP NANOHEX | | | | 2610038-00 | 7 |
| J2 | J1 | | | | | | |
| J3 | J1 | | | | | | |
| J4 | J1 | | | | | | |
| J5 | J17 | | | | | | |
| J6 | J1 | | | | | | |
| J7 | J1 | | | | | | |
| L1 | | INDUCTOR,SMD,.033µH | | | | 3530025-05 | 5 |
| L2 | | INDUCTOR,SMD,.082µH | | | | 3530025-32 | 1 |
| L3 | L1 | | | | | | |
| L4 | L1 | | | | | | |
| L5 | L1 | | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-02 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| L6 | L1 | | | | | | |
| L7 | | INDUCTOR,SMD,2.2µH | | | | 3530025-16 | 1 |
| L8 | | INDUCTOR,SMD,.100µH | | | | 3530025-08 | 1 |
| L9 | | INDUCTOR,SMD,1.5µH | | | | 3530025-15 | 1 |
| L10 | | INDUCTOR,SMD,180µH | | | | 3530024-03 | 1 |
| Q1 | | XSTR,SMD,MMBF4416,SOT-23 | | | | 4730014-00 | 1 |
| Q2 | | XSTR,MMBT3960,NPN SWITCHING | | | | 1410101-00 | 1 |
| R1 | | RES,SMD | 56.2 | 1/8W | 1% | 4235629-00 | 2 |
| R2 | | RES,SMD | 22.1 | 1/8W | 1% | 4232219-00 | 3 |
| R3 | R2 | | | | | | |
| R4 | | RES,SMD | 100 | 1/8W | 1% | 4231000-00 | 11 |
| R5 | R4 | | | | | | |
| R6 | | RES,SMD | 10.0 | 1/8W | 1% | 4231009-00 | 11 |
| R7 | | RES,SMD | 562 | 1/8W | 1% | 4235620-00 | 2 |
| R8 | | RES,SMD | 6.81K | 1/8W | 1% | 4236811-00 | 1 |
| R9 | | RES,SMD | 1K | 1/8W | 1% | 4231001-00 | 9 |
| R10 | R7 | | | | | | |
| R11 | R9 | | | | | | |
| R12 | R4 | | | | | | |
| R13 | R6 | | | | | | |
| R14 | R4 | | | | | | |
| R15 | | RES,SMD | 68.1 | 1/8W | 1% | 4236819-00 | 2 |
| R16 | R6 | | | | | | |
| R17 | R15 | | | | | | |
| R18 | | RES,SMD | 681 | 1/8W | 1% | 4236810-00 | 4 |
| R19 | | RES,SMD | 2.21K | 1/8W | 1% | 4232211-00 | 5 |
| R20 | R6 | | | | | | |
| R21 | R4 | | | | | | |
| R22 | R4 | | | | | | |
| R23 | R6 | | | | | | |
| R24 | R4 | | | | | | |
| R25 | R4 | | | | | | |
| R26 | R19 | | | | | | |
| R27 | R19 | | | | | | |
| R28 | R18 | | | | | | |
| R29 | | RES,SMD | 511 | 1/8W | 1% | 4235110-00 | 8 |
| R30 | R2 | | | | | | |
| R31 | | RES,SMD | 221 | 1/8W | 1% | 4232210-00 | 6 |
| R32 | | RES,SMD | 82.5 | 1/8W | 1% | 4238259-00 | 1 |
| R33 | R4 | | | | | | |
| R34 | R18 | | | | | | |
| R35 | | RES,SMD | 1.10K | 1/8W | 1% | 4231101-00 | 1 |
| R36 | | RES,SMD | 825 | 1/8W | 1% | 4238250-00 | 2 |
| R37 | R1 | | | | | | |
| R38 | | NOT USED | | | | | |
| R39 | R6 | | | | | | |
| R40 | R31 | | | | | | |
| R41 | R6 | | | | | | |
| R42 | | RES,SMD | 301 | 1/8W | 1% | 4233010-00 | 3 |
| R43 | | RES,SMD | 10K | 1/8W | 1% | 4231002-00 | 4 |
| R44 | R31 | | | | | | |
| R45 | | RES,SMD | 475 | 1/8W | 15 | 4234750-00 | 4 |
| R46 | R45 | | | | | | |
| R47 | R45 | | | | | | |
| R48 | | RES,SMD | 332 | 1/8W | 1% | 4233320-00 | 7 |
| R49 | R9 | | | | | | |
| R50 | R45 | | | | | | |
| R51 | R9 | | | | | | |
| R52 | R48 | | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-02 Rev. D

| REF DES. | SAME AS | DESCRIPTION | | | | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|---|---|---|
| R53 | R48 | | | | | | |
| R54 | R48 | | | | | | |
| R55 | R19 | | | | | | |
| R56 | R48 | | | | | | |
| R57 | | RES,SMD | 4.75K | 1/8W | 1% | 4234751-00 | 1 |
| R58 | | RES,SMD | 47.5 | 1/8W | 1% | 4234759-00 | 1 |
| R59 | R31 | | | | | | |
| R60 | R48 | | | | | | |
| R61 | R48 | | | | | | |
| R62 | R43 | | | | | | |
| R63 | | RES,SMD | 4.32K | 1/8W | 1% | 4234321-00 | 2 |
| R64 | R4 | | | | | | |
| R65 | R29 | | | | | | |
| R66 | | RES,SMD | 3.32K | 1/8W | 1% | 4233321-00 | 1 |
| R67 | R43 | | | | | | |
| R68 | | RES,SMD | 47.5K | 1/8W | 1% | 4234752-00 | 1 |
| R69 | R9 | | | | | | |
| R70 | R18 | | | | | | |
| R71 | R9 | | | | | | |
| R72 | | JUMPER,SMD,MINI MCR18 | | | | 5000288-00 | 5 |
| R73 | | RES,SMD | 1.82K | 1/8W | 1% | 4231821-00 | 1 |
| R74 | R36 | | | | | | |
| R75 | | RES,SMD | 365 | 1/8W | 1% | 4233650-00 | 1 |
| R76 | | RES,SMD | 182 | 1/8W | 1% | 4231820-00 | 1 |
| R77 | R43 | | | | | | |
| R78 | R9 | | | | | | |
| R79 | R9 | | | | | | |
| R80 | R72 | | | | | | |
| R81 | | RES,SMD | 2.00K | 1/8W | 1% | 4232001-00 | 1 |
| R82 | | RES,SMD | 750 | 1/8W | 1% | 4237500-00 | 1 |
| R83 | R31 | | | | | | |
| R84 | | RES,SMD | 130 | 1/8W | 1% | 4231300-00 | 1 |
| R85 | R9 | | | | | | |
| R86 | | RES,SMD | 5.11K | 1/8W | 1% | 4235111-00 | 1 |
| R87 | R4 | | | | | | |
| R88 | R42 | | | | | | |
| R89 | R42 | | | | | | |
| R90 | R72 | | | | | | |
| R91 | | RES,SMD | 100K | 1/8W | 1% | 4231003-00 | 1 |
| R92 | | RES,SMD | 1.00M | 1/8W | 1% | 4231004-00 | 1 |
| R93 | | RES,SMD | 10.0M | 1/8W | 1% | 4231005-00 | 1 |
| R94 | R6 | | | | | | |
| R95 | | RES,SMD | 1.50K | 1/8W | 1% | 4231501-00 | 1 |
| R96 | R6 | | | | | | |
| R97 | R6 | | | | | | |
| R98 | R29 | | | | | | |
| R99 | R6 | | | | | | |
| R100 | R19 | | | | | | |
| R101 | R29 | | | | | | |
| R102 | R29 | | | | | | |
| R103 | R29 | | | | | | |
| R104 | | RES,SMD | 619 | 1/8W | 1% | 4236190-00 | 1 |
| R105 | | RES,SMD | 2.74K | 1/8W | 1% | 4232741-00 | 1 |
| R106 | R29 | | | | | | |
| R107 | R31 | | | | | | |
| R108 | R63 | | | | | | |
| R109 | R29 | | | | | | |
| TP1 | | NOT USED | | | | | |
| TP2 | | NOT USED | | | | | |
| TP3 | | NOT USED | | | | | |
| TP4 | | NOT USED | | | | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-02 Rev. D

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| TP5 | | NOT USED | | |
| TP6 | | NOT USED | | |
| TP7 | | NOT USED | | |
| TP8 | | NOT USED | | |
| TP9 | | NOT USED | | |
| TP10 | | NOT USED | | |
| TP11 | | NOT USED | | |
| TP12 | | NOT USED | | |
| TP1 | | NOT USED | | |
| TP14 | | NOT USED | | |
| TP15 | | NOT USED | | |
| U1 | | IC,SMD,MSA-0385,MMIC | 3170071-00 | 4 |
| U2 | U1 | | | |
| U3 | | IC,SMD,MSA-0885,AMP MMIC | 5352005-00 | 1 |
| U4 | U1 | | | |
| U5 | U1 | | | |
| U6 | | IC,SMD,10H124,TTL/MECL TRANSLATOR | 3170072-00 | 1 |
| U7 | | IC,SMD,10H104,MECL AND GATES | 3170073-00 | 1 |
| U8 | | IC,3199E,VHF/UHF,4 PRESCALER | 3043199-00 | 1 |
| U9 | | IC,AD96685,ULTRAFAST COMPARATOR | 3110126-00 | 1 |
| U10 | | IC,SMD,74HC595,8-BIT SHIFT REGISTER | 3170056-00 | 2 |
| U11 | | IC,SMD,DG403DY | 3110130-00 | 2 |
| U12 | U11 | | | |
| U13 | | IC,AD1856,16-BIT PCM AUDIO DAC | 3110129-00 | 1 |
| U14 | | IC,SMD,OP-27,OP AMPL,S08 | 3170045-00 | 3 |
| U15 | U14 | | | |
| U16 | | IC,SMD,NE521 | 3170028-00 | 4 |
| U17 | U16 | | | |
| U18 | U14 | | | |
| U19 | U16 | | | |
| U20 | U16 | | | |
| U21 | | PAL,PRGM,16L8,DECODER | 2070086-00 | 1 |
| U22 | | IC,SMD,74LS279A,QUAD S-R FF | 3170080-00 | 2 |
| U23 | U22 | | | |
| U24 | | IC,SMD,74HC165,SHIFT REGISTER | 3170078-00 | 1 |
| U25 | U10 | | | |
| U26 | | IC,SMD,74S00,QUAD 2-INPUT NAND GATE | 3170079-00 | 1 |
| U27 | | IC,SMD.74HC125,QUAD 3-STATE | 3110127-00 | 1 |
| U28 | | IC,SMD,10H125,MECL/TTL TRANSLATOR | 3170070-00 | 1 |
| U29 | | IC,SMD,10216,H,SP TPL LINE RX | 3170034-00 | 1 |
| W1 | | NOT USED | | |
| W2 | | NOT USED | | |
| W3 | R72 | | | |
| W4 | R72 | | | |
| XU1 | | NOT USED | | |
| XU2 | | NOT USED | | |
| XU3 | | NOT USED | | |
| XU4 | | NOT USED | | |
| XU5 | | NOT USED | | |
| XU6 | | NOT USED | | |
| XU7 | | NOT USED | | |
| XU8 | | CONN,SOCKET,DIP,8 PIN | 2630014-00 | 1 |
| XU9 | | NOT USED | | |
| XU10 | | NOT USED | | |
| XU11 | | NOT USED | | |
| XU12 | | NOT USED | | |
| XU13 | | NOT USED | | |
| XU14 | | NOT USED | | |
| XU15 | | NOT USED | | |

## A9 SIGNAL CONDITIONER (Continued) 2020420-02 Rev. D

| REF DES. | SAME AS | DESCRIPTION | EIP NO. | UNITS PER ASSY |
|---|---|---|---|---|
| XU16 | | NOT USED | | |
| XU17 | | NOT USED | | |
| XU18 | | NOT USED | | |
| XU19 | | NOT USED | | |
| XU20 | | NOT USED | | |
| XU21 | | CONN,SOCKET,DIP,20 PIN | 2630018-00 | 1 |
| XU22 | | NOT USED | | |
| XU23 | | NOT USED | | |
| XU24 | | NOT USED | | |
| XU25 | | NOT USED | | |
| XU26 | | NOT USED | | |
| XU27 | | NOT USED | | |
| XU28 | | NOT USED | | |
| XU29 | | NOT USED | | |
| HARDWARE USED IN THIS ASSEMBLY | | | | |
| | | HANDLE,PCB | 5230001-00 | 2 |
| | | PIN,ROLL,3/32 DIA 1/4 LG | 5110008-00 | 2 |
| | | WIRE,INSUL,18AWG GRN | 5418555-00 | 1 |
| | | PCB SCHEMATIC DIAGRAM | 5500420-02 B | REF. |

## COMPONENT COORDINATES (SIGNAL CONDITIONER ASSEMBLY A9)

| REF DES | COORD | REF DES | COORD | REF DES | COORD | REF DES | COORD | REF DES | COORD |
|---|---|---|---|---|---|---|---|---|---|
| C1 | A-1 | C60 | B-8 | L1 | A-1 | R45 | A-3 | R103 | C-12 |
| C2 | A-2 | C61 | B-7 | L2 | A-2 | R46 | A-3 | R104 | C-12 |
| C3 | A-2 | C62 | B-7 | L3 | B-1 | R47 | A-3 | R105 | D-12 |
| C4 | A-2 | C63 | B-8 | L4 | C-1 | R48 | B-4 | R106 | D-11 |
| C5 | B-1 | C64 | B-2 | L5 | D-1 | R49 | B-4 | R107 | D-11 |
| C6 | B-1 | C65 | C-7 | L6 | D-2 | R50 | B-4 | R108 | D-12 |
| C7 | B-2 | C66 | C-8 | L7 | D-2 | R51 | C-3 | R109 | D-12 |
| C8 | B-2 | C67 | A-9 | L8 | C-3 | R52 | C-3 | | |
| C9 | C-1 | C68 | B-9 | L9 | D-2 | R53 | C-4 | TP1 | A-1 |
| C10 | C-2 | C69 | B-9 | L10 | B-7 | R54 | C-3 | TP2 | A-1 |
| C11 | C-1 | C70 | C-9 | | | R55 | C-4 | TP3 | B-2 |
| C12 | C-2 | C71 | C-9 | Q1 | B-12 | R56 | C-4 | TP4 | C-2 |
| C13 | D-1 | C72 | C-9 | Q2 | B-12 | R57 | C-3 | TP5 | C-1 |
| C14 | D-2 | C73 | C-9 | | | R58 | C-3 | TP6 | D-1 |
| C15 | B-2 | C74 | C-9 | R1 | A-2 | R59 | C-4 | TP7 | D-3 |
| C16 | C-2 | C75 | A-10 | R2 | A-2 | R60 | C-3 | TP8 | A-4 |
| C17 | D-2 | C76 | B-10 | R3 | A-2 | R61 | C-4 | TP9 | C-5 |
| C18 | A-3 | C77 | B-11 | R4 | A-1 | R62 | D-4 | TP10 | D-5 |
| C19 | B-2 | C78 | B-11 | R5 | A-1 | R63 | D-4 | TP11 | B-7 |
| C20 | B-3 | C79 | A-12 | R6 | A-1 | R64 | B-5 | TP12 | C-9 |
| C21 | C-3 | C80 | A-12 | R7 | A-1 | R65 | B-5 | TP13 | A-11 |
| C22 | C-2 | C81 | B-12 | R8 | B-1 | R66 | B-5 | TP14 | D-11 |
| C23 | C-2 | C82 | B-11 | R9 | B-1 | R67 | C-5 | TP15 | D-12 |
| C24 | C-2 | C83 | B-12 | R10 | B-1 | R68 | C-5 | | |
| C25 | D-3 | C84 | C-11 | R11 | B-2 | R69 | C-5 | U1 | A-2 |
| C26 | D-3 | C85 | C-12 | R12 | B-1 | R70 | C-5 | U2 | B-2 |
| C27 | B-2 | C86 | C-11 | R13 | B-1 | R71 | C-5 | U3 | C-2 |
| C28 | D-3 | C87 | C-12 | R14 | B-1 | R72 | A-7 | U4 | D-2 |
| C29 | C-3 | C88 | D-11 | R15 | C-1 | R73 | A-7 | U5 | C-2 |
| C30 | B-3 | C89 | D-12 | R16 | C-1 | R74 | A-8 | U6 | B-3 |
| C31 | B-3 | C90 | D-11 | R17 | C-1 | R75 | A-8 | U7 | B-3 |
| C32 | C-4 | C91 | B-12 | R18 | C-2 | R76 | A-8 | U8 | C-3 |
| C33 | C-3 | C92 | C-11 | R19 | C-2 | R77 | A-8 | U9 | D-3 |
| C34 | D-3 | | | R20 | C-1 | R78 | B-7 | U10 | A-4 |
| C35 | C-3 | CR1 | B-1 | R21 | C-1 | R79 | B-7 | U11 | B-4 |
| C36 | D-3 | CR2 | B-2 | R22 | C-2 | R80 | B-7 | U12 | C-4 |
| C37 | A-4 | CR3 | B-2 | R23 | D-1 | R81 | B-8 | U13 | A-5 |
| C38 | B-4 | CR4 | C-2 | R24 | D-1 | R82 | B-8 | U14 | B-5 |
| C39 | B-5 | CR5 | C-2 | R25 | D-1 | R83 | A-8 | U15 | C-5 |
| C40 | C-4 | CR6 | C-2 | R26 | B-2 | R84 | A-8 | U16 | A-7 |
| C41 | C-5 | CR7 | C-2 | R27 | B-2 | R85 | B-2 | U17 | A-8 |
| C42 | D-4 | CR8 | C-2 | R28 | C-2 | R86 | B-7 | U18 | B-2 |
| C43 | D-4 | CR9 | C-2 | R29 | C-2 | R87 | B-7 | U19 | B-8 |
| C44 | D-5 | CR10 | D-2 | R30 | D-2 | R88 | B-8 | U20 | B-8 |
| C45 | A-5 | CR11 | B-2 | R31 | D-2 | R89 | B-8 | U21 | C-7 |
| C46 | B-5 | CR12 | B-2 | R32 | A-3 | R90 | A-11 | U22 | A-9 |
| C47 | B-5 | CR13 | C-4 | R33 | B-3 | R91 | A-12 | U23 | B-9 |
| C48 | B-5 | CR14 | B-12 | R34 | B-3 | R92 | A-12 | U24 | C-9 |
| C49 | B-6 | CR15 | A-12 | R35 | B-3 | R93 | B-11 | U25 | A-10 |
| C50 | C-5 | CR16 | A-12 | R36 | B-2 | R94 | B-11 | U26 | B-10 |
| C51 | C-5 | | | R37 | C-3 | R95 | B-12 | U27 | C-10 |
| C52 | C-5 | J1 | A-2 | R38 | C-2 | R96 | B-12 | U28 | A-11 |
| C53 | C-5 | J2 | B-2 | R39 | C-3 | R97 | B-11 | U29 | D-11 |
| C54 | A-7 | J3 | A-3 | R40 | C-2 | R98 | B-12 | | |
| C55 | A-7 | J4 | B-3 | R41 | B-3 | R99 | B-12 | W1 | C-10 |
| C56 | A-9 | J5 | A-4 | R42 | D-2 | R100 | C-12 | W2 | C10 |
| C57 | A-8 | J6 | A-7 | R43 | D-3 | R101 | C-11 | W3 | C-10 |
| C58 | B-7 | J7 | A-11 | R44 | D-3 | R102 | C-11 | W4 | C-10 |
| C59 | B-8 | | | | | | | | |

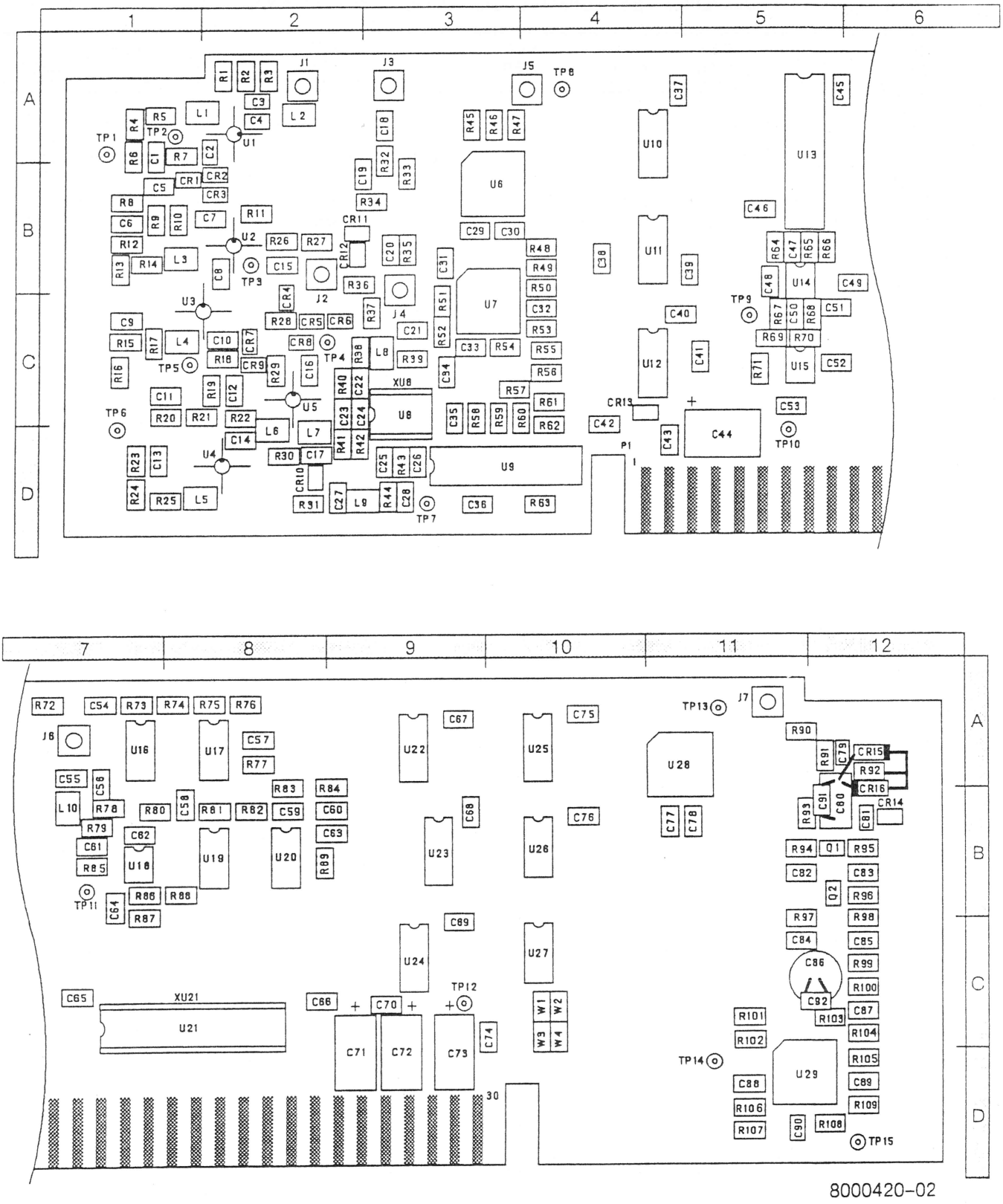
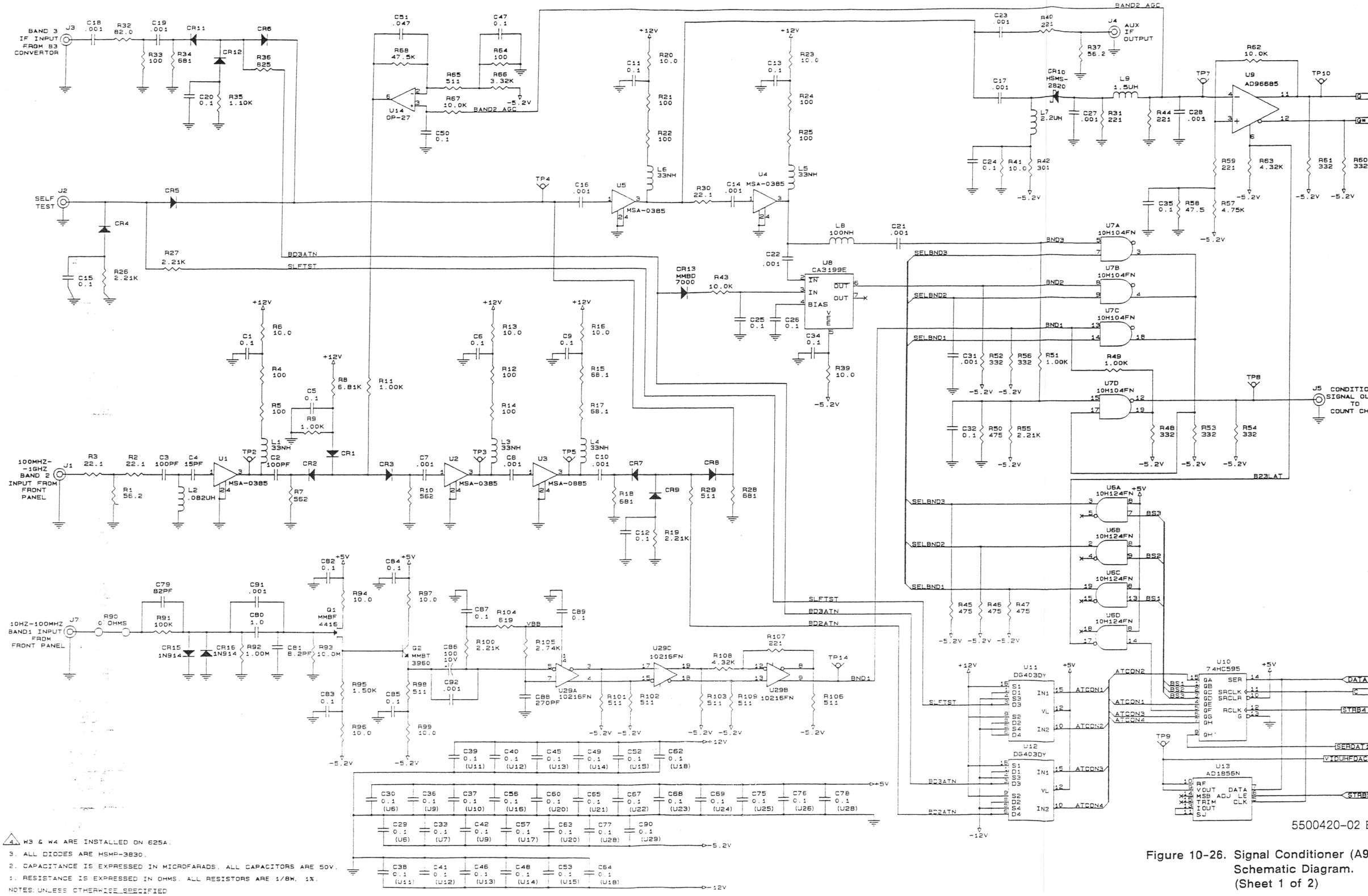



Figure 10-25. Signal Conditioner (A9) Component Locator.

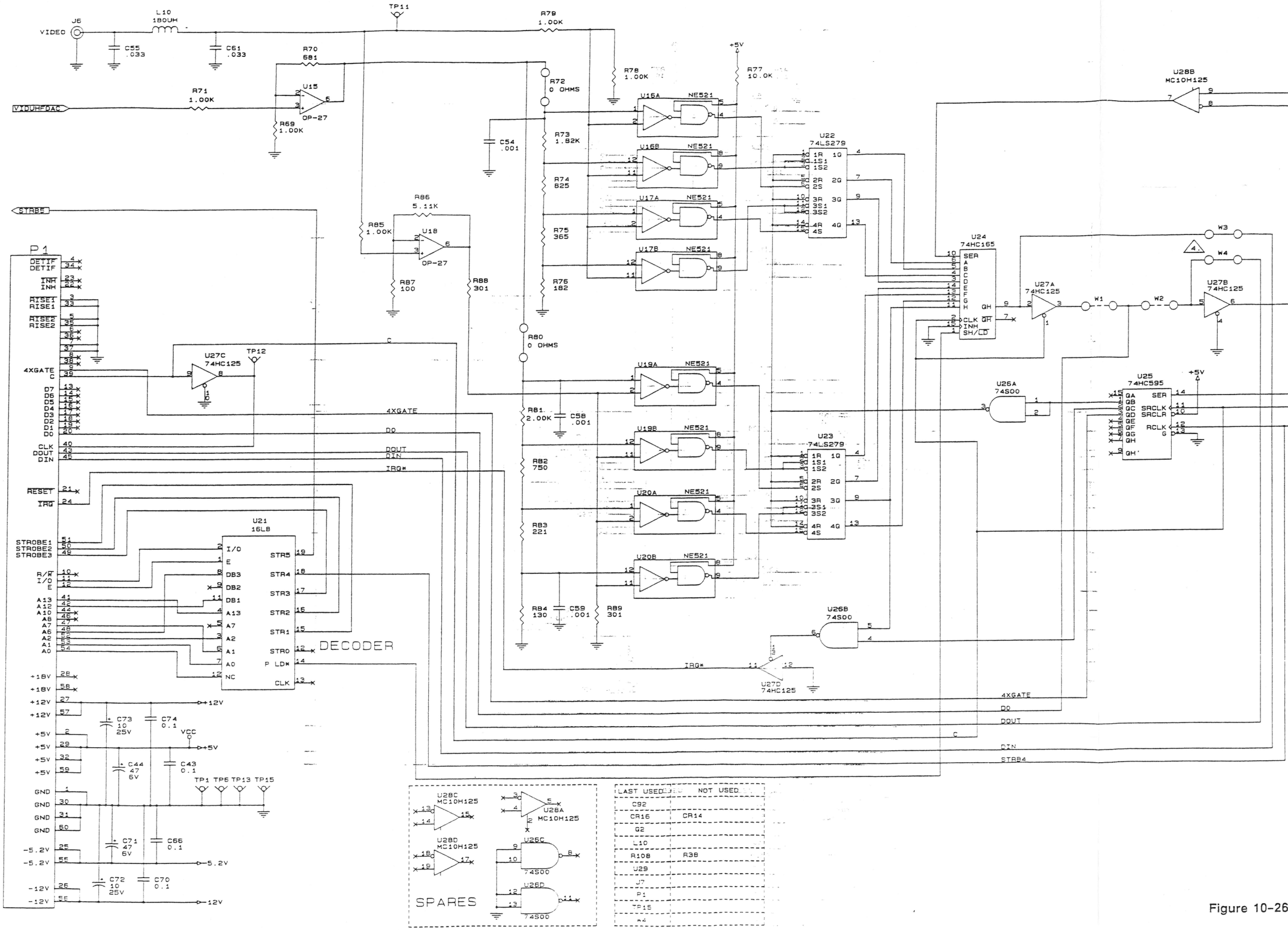



4. W3 & W4 ARE INSTALLED ON 625A.
3. ALL DIODES ARE HSMP-3830.
2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 50V.
1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W. 1%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500420-02 E

Figure 10-26. Signal Conditioner (A9 Schematic Diagram. (Sheet 1 of 2)




| LAST USED | NOT USED |
|---|---|
| C92 | |
| CR16 | CR14 |
| G2 | |
| L10 | |
| R108 | R38 |
| U29 | |
| J7 | |
| P1 | |
| TP15 | |
| R4 | |

IC POWER TABLE

| IC NO. | IC PINS | | | |
|---|---|---|---|---|
| | GND | +5V | -5.2V | +12V |
| U1 | 2, 4 | | | |
| U2 | 2, 4 | | | |
| U3 | 2, 4 | | | |
| U4 | 2, 4 | | | |
| U5 | 2, 4 | | | |
| U6 | 20 | 12 | 10 | |
| U7 | 2, 20 | | 10 | |
| U8 | 8 | | (5) | |
| U9 | 1, 16 | 2 | 8 | |
| U10 | 8 | 16 | | |
| U11 | 13 | 12 | | 11 |
| U12 | 13 | 12 | | 11 |
| U13 | 2, 12 | | | 3, 16 |
| U14 | | | | 7 |
| U15 | | | | 7 |
| U16 | 7 | 6, 14 | 13 | |
| U17 | 7 | 6, 14 | 13 | |
| U18 | | | | 7 |
| U19 | 7 | 6, 14 | 13 | |
| U20 | 7 | 6, 14 | 13 | |
| U21 | 10 | 20 | | |
| U22 | 8 | 16 | | |
| U23 | 8 | 16 | | |
| U24 | 8 | 16 | | |
| U25 | 8 | 16 | | |
| U26 | 7 | 14 | | |
| U27 | 7 | 14 | | |
| U28 | 20 | 12 | 10 | |
| U29 | 2, 20 | | 10 | |

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Figure 10-26. Signal Conditioner (A
Schematic Diagram.
(Sheet 2 of 2)

REV. 10/25/90

10-73/10-74

BACKDATE 5580076-00